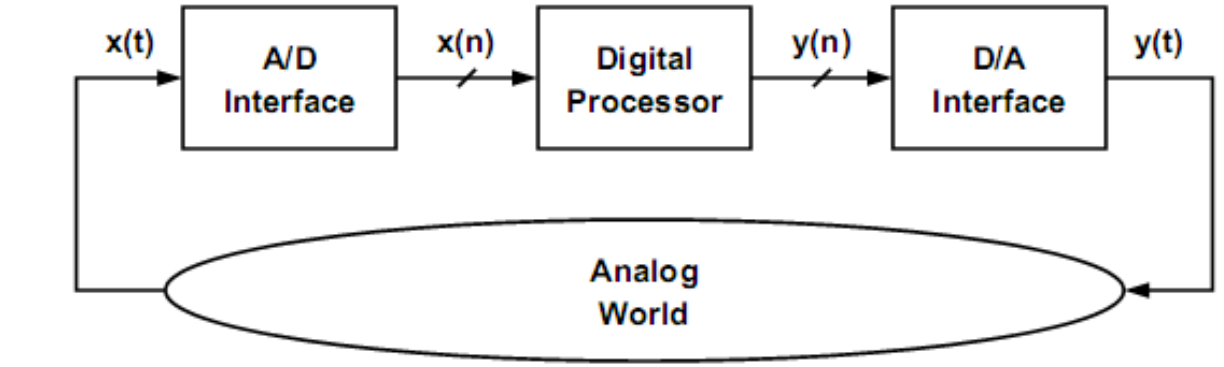
Analog-to-Digital converters

Apinunt Thanachayanont

A/D and D/A interfaces



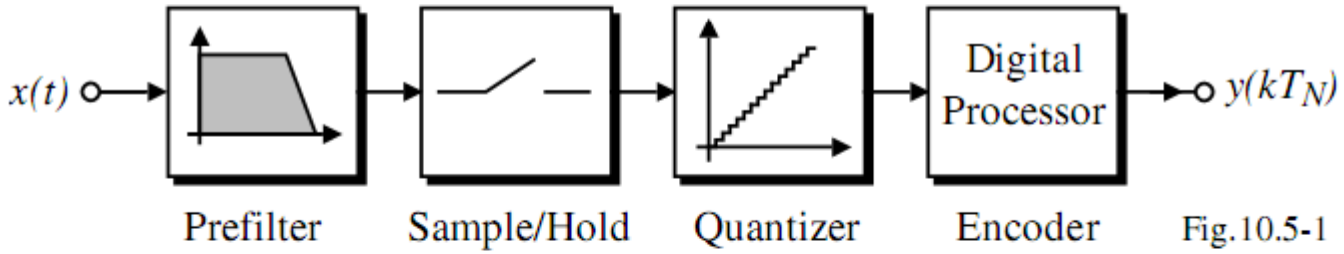


Fig.10.5-1

- Prefilter - Avoids the aliasing of high frequency signals back into the baseband of the ADC
- Sample-and-hold - Maintains the input analog signal constant during conversion
- Quantizer - Finds the subrange that corresponds to the sampled analog input
- Encoder - Encoding of the digital bits corresponding to the subrange

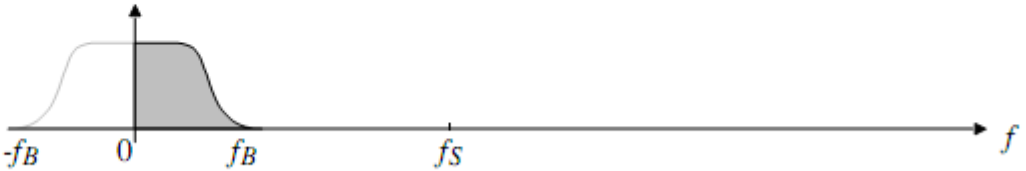
Nyquist frequency: ADC

The sampled nature of the ADC places a practical limit on the bandwidth of the input signal. If the sampling frequency is f_S, and f_B is the bandwidth of the input signal, then

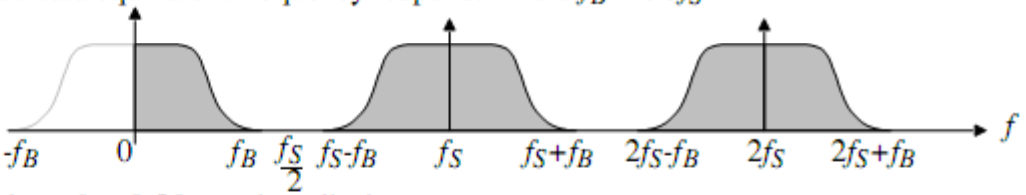
$$f_B < 0.5f_S$$

which is simply the *Nyquist* relationship which states that to avoid aliasing, the sampling frequency must be greater than twice the highest signal frequency.

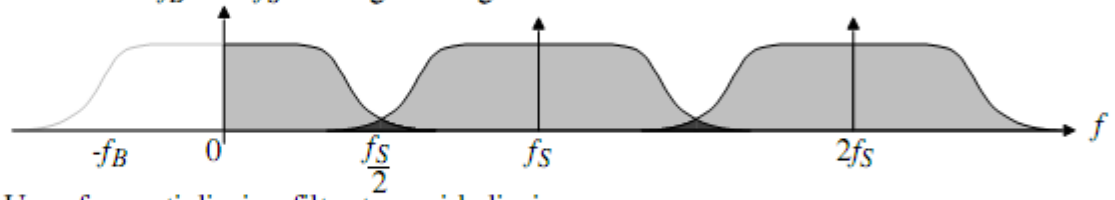
Continuous time frequency response of the analog input signal.



Sampled data equivalent frequency response where $f_B < 0.5f_S$.



Case where $f_B > 0.5f_S$ causing aliasing.



Use of an antialiasing filter to avoid aliasing.

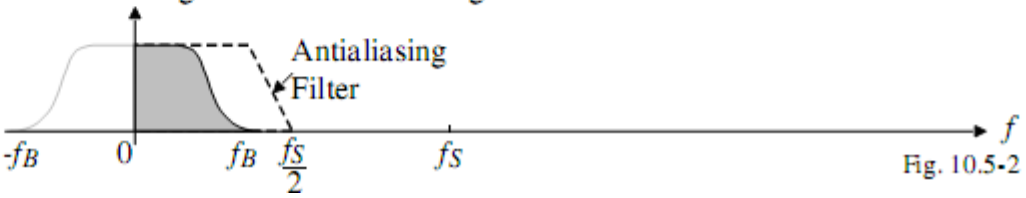


Fig. 10.5-2

Types of ADCs

Analog-digital converters can be classified by the relationship of f_B and $0.5f_S$ and by their conversion rate.

- *Nyquist ADCs* - ADCs that have f_B as close to $0.5f_S$ as possible.
- *Oversampling ADCs* - ADCs that have f_B much less than $0.5f_S$.

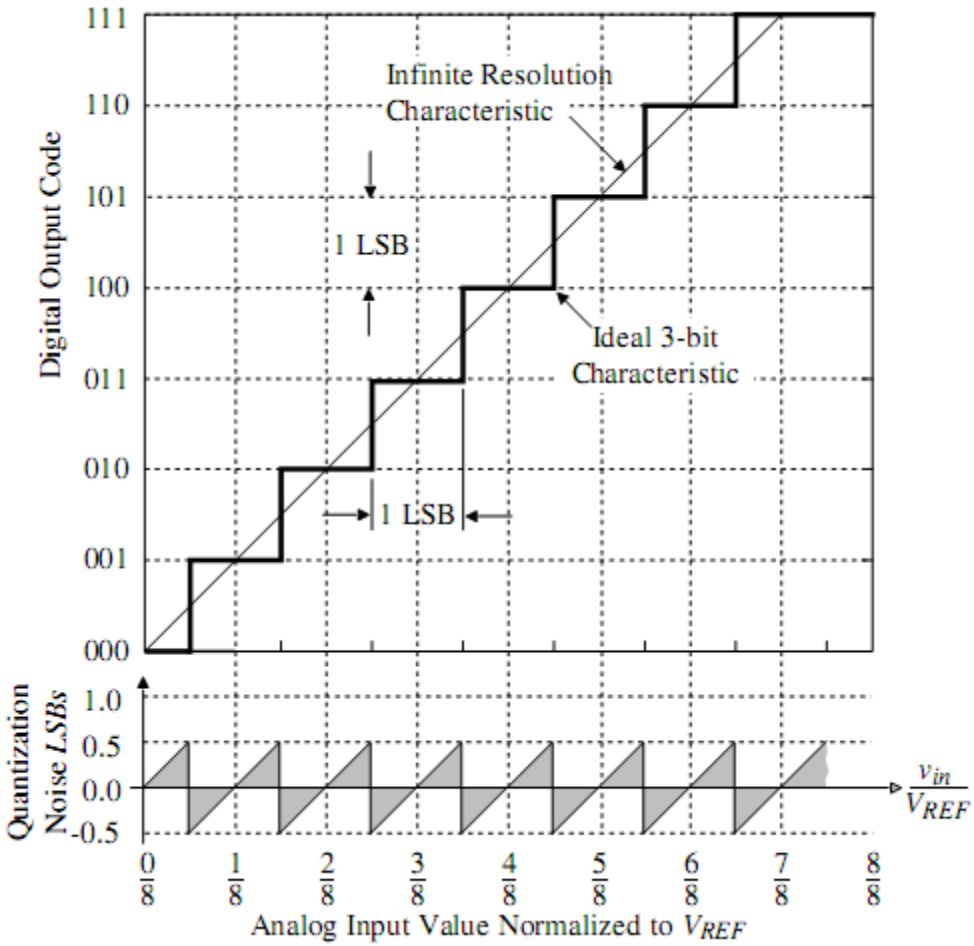
Table 10.5-1 - Classification of Analog-to-Digital Converter Architectures

Conversion Rate	Nyquist ADCs	Oversampled ADCs
Slow	Integrating (Serial)	Very high resolution >14 bits
Medium	Successive Approximation1-bit Pipeline Algorithmic	Moderate resolution >10 bits
Fast	Flash Multiple-bit Pipeline Folding and interpolating	Low resolution > 6 bits

Digital output codes

Decimal	Binary	Thermometer	Gray	Two's Complement
0	000	0000000	000	000
1	001	0000001	001	111
2	010	0000011	011	110
3	011	0000111	010	101
4	100	0001111	110	100
5	101	0011111	111	011
6	110	0111111	101	010
7	111	1111111	100	001

Input-output characteristic of ADC



Static characteristics

- The *dynamic range, signal-to-noise ratio (SNR)*, and the *effective number of bits (ENOB)* of the ADC are the same as for the DAC
- *Resolution* of the ADC is the smallest analog change that distinguishable by an ADC.
- *Quantization Noise* is the $\pm 0.5LSB$ uncertainty between the infinite resolution characteristic and the actual characteristic.
- *Offset Error* is the difference between the ideal finite resolution characteristic and actual finite resolution characteristic
- *Gain Error* is the difference between the ideal finite resolution charact-eristic and actual finite resolution characteristic measured at full-scale input. This difference is *proportional* to the analog input voltage.

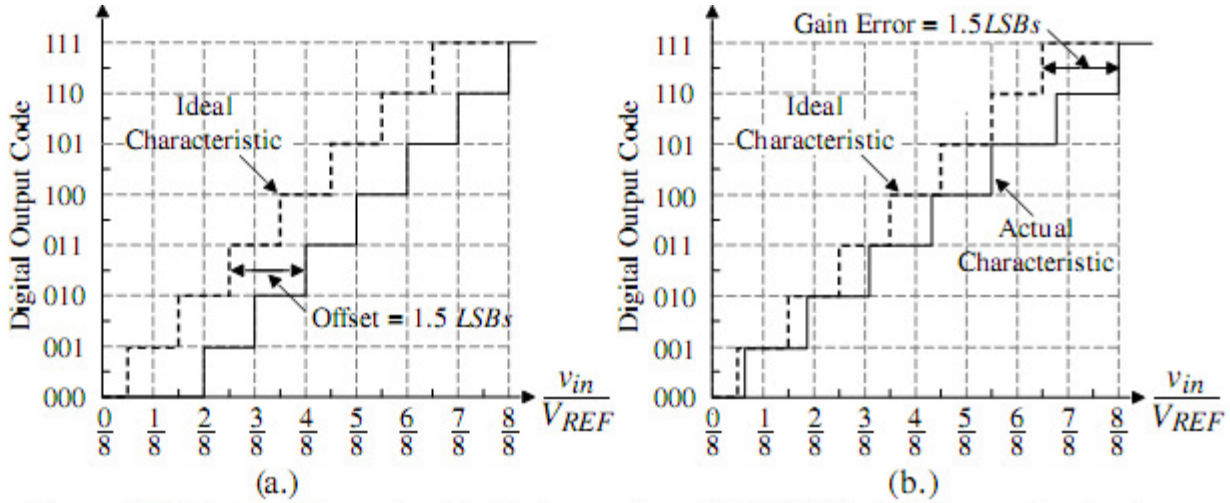


Figure 10.5-4 - (a.) Example of offset error for a 3-bit ADC. (b.) Example of gain error for a 3-bit ADC.

INL & DNL

The integral and differential nonlinearity of the ADC are referenced to the vertical (digital) axis of the transfer characteristic.

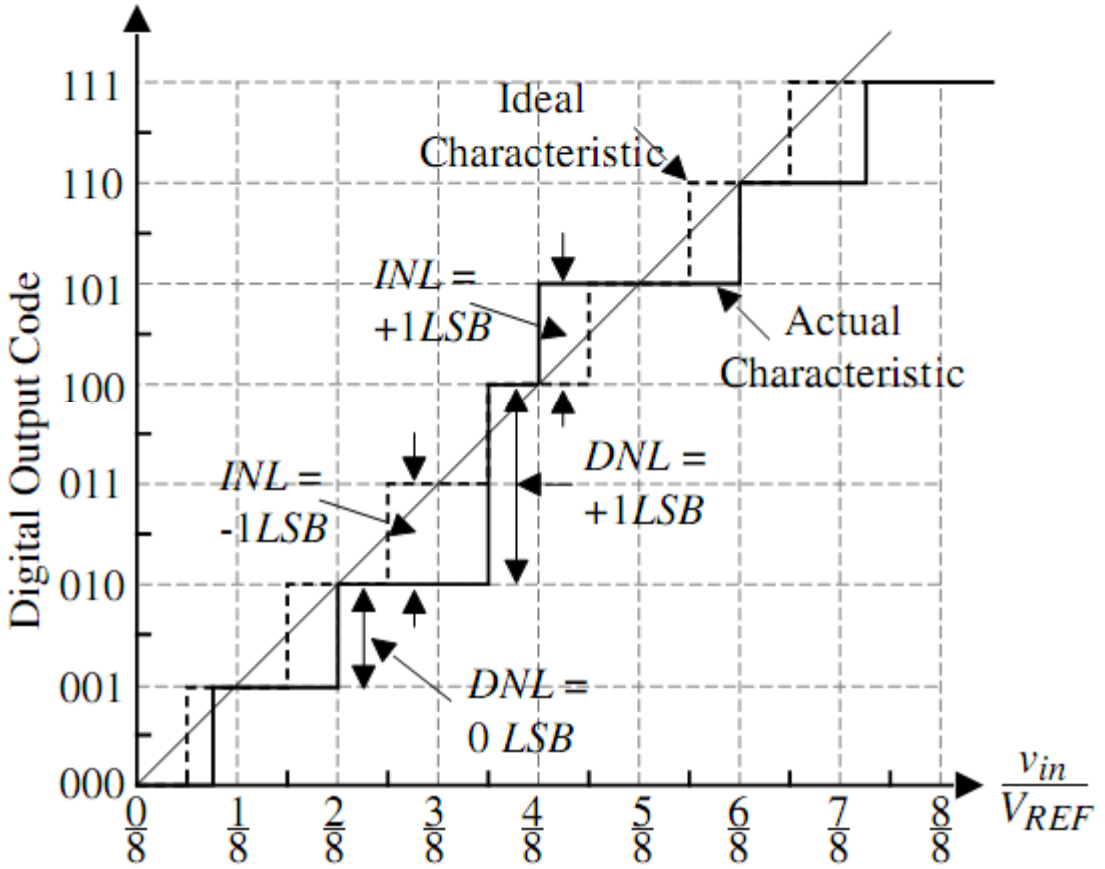
- *Integral Nonlinearity (INL)* is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically (% or *LSB*)
- *Differential Nonlinearity (DNL)* is a measure of the separation between adjacent levels measured at each vertical step (% or *LSB*).

$$DNL = (D_{cx} - 1)\ LSBs$$

where D_{cx} is the size of the actual vertical step in *LSBs*.

Note that *INL* and *DNL* of an analog-digital converter will be in terms of integers in contrast to the *INL* and *DNL* of the digital-analog converter. As the resolution of the ADC increases, this restriction becomes insignificant.

Example of INL &DNL



Example of *INL* and *DNL* for a 3-bit ADC.) Fig.10.5-5

Monotonicity

A *monotonic* ADC has all vertical jumps positive. Note that monotonicity can only be detected by *DNL*.

Example of a nonmonotonic ADC:

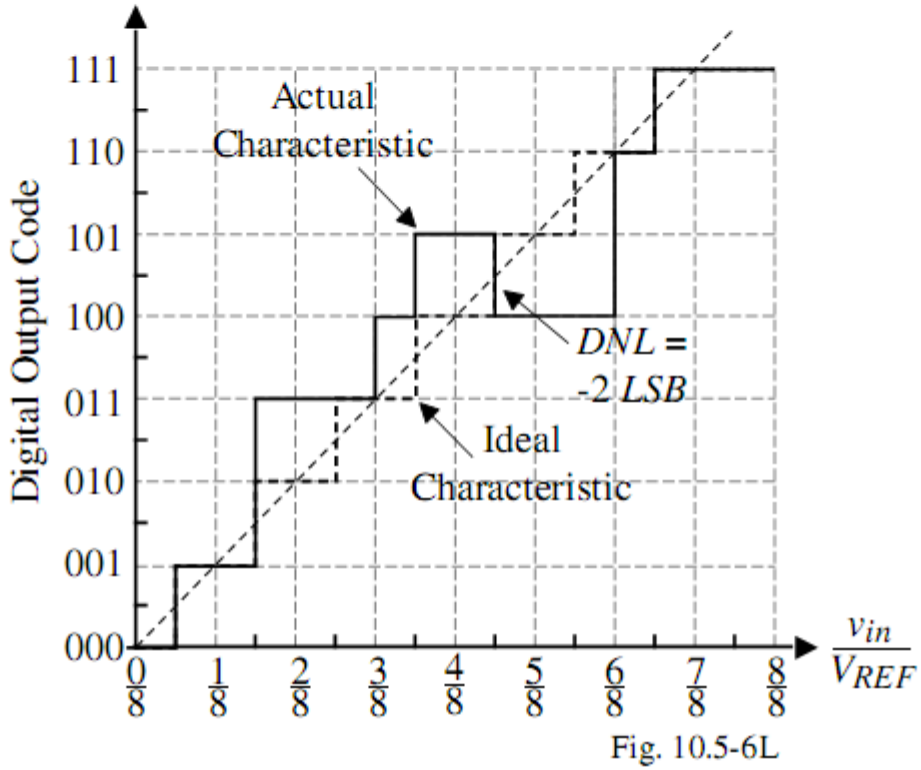
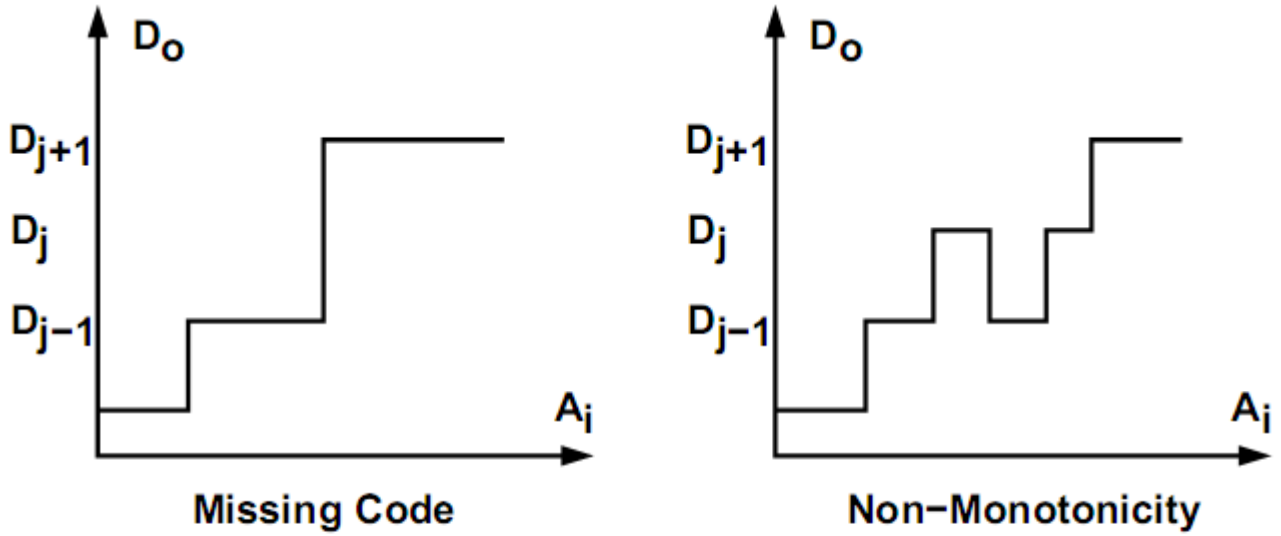


Fig. 10.5-6L

If a vertical jump is 2*LSB* or greater, missing output codes may result.

If a vertical jump is -1*LSB* or less, the ADC is not monotonic.

Missing Code and Non-Monotonicity



- If DNL = −1 LSB, a code is missing.
- Missing code, non-monotonicity, and DNL near the operating point come out when small signal trips over them. Critical in control and video.
- Dithering is effective to smooth out DNL by spreading it over neighboring codes.

INL & DNL of 3-bit ADC

Find the *INL* and *DNL* for the 3-bit ADC shown on the previous slide.

Solution

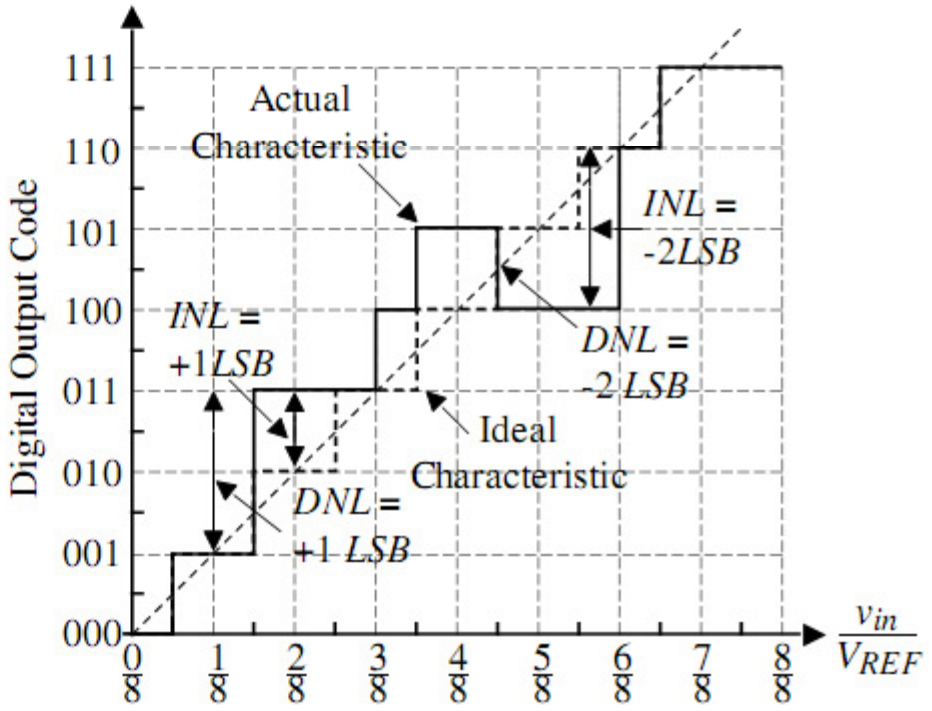
With respect to the digital axis:

1.) The largest value of *INL* for this 3-bit ADC occurs between 3/16 to 5/16 or 7/16 to 9/16 and is 1*LSB*.

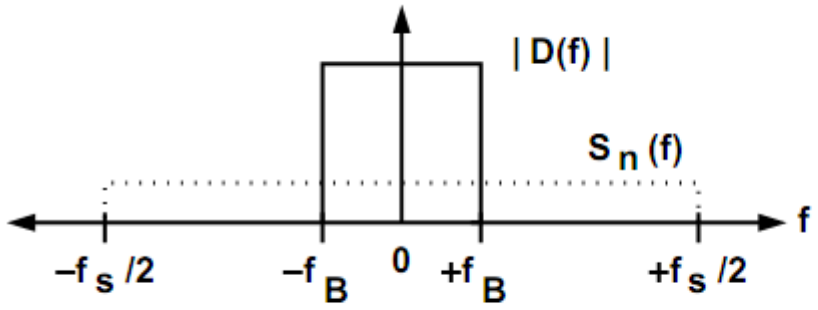
2.) The smallest value of *INL* occurs between 11/16 to 12/16 and is -2*LSB*.

3.) The largest value of *DNL* occurs at 3/16 or 6/8 and is +1*LSB*.

4.) The smallest value of *DNL* occurs at 9/16 and is -2*LSB* which is where the converter becomes nonmonotonic.



Oversampling



$$\text{SNR} = \frac{S}{N}$$

$$N = \int_{-f_s/2}^{+f_s/2} S_n(f)df$$

If input signal is band-limited between $\pm f_B$, by putting the ADC's output through a digital low-pass filter with f_B bandwidth, the remaining noise is

$$N' = \int_{-f_B/2}^{+f_B/2} S_n(f)df = \frac{N}{M} \qquad \text{Oversampling Ratio} = M \equiv \frac{f_s/2}{f_B}$$

Since the desired signal is unchanged, we have

$$\text{SNR}' = M \times \text{SNR}$$

Serial ADC

Serial ADCs typically require $2^N T$ for conversion where T = period of the clock

Types:

- Single-slope
- Dual-slope

Single-Slope ADC

Block diagram:

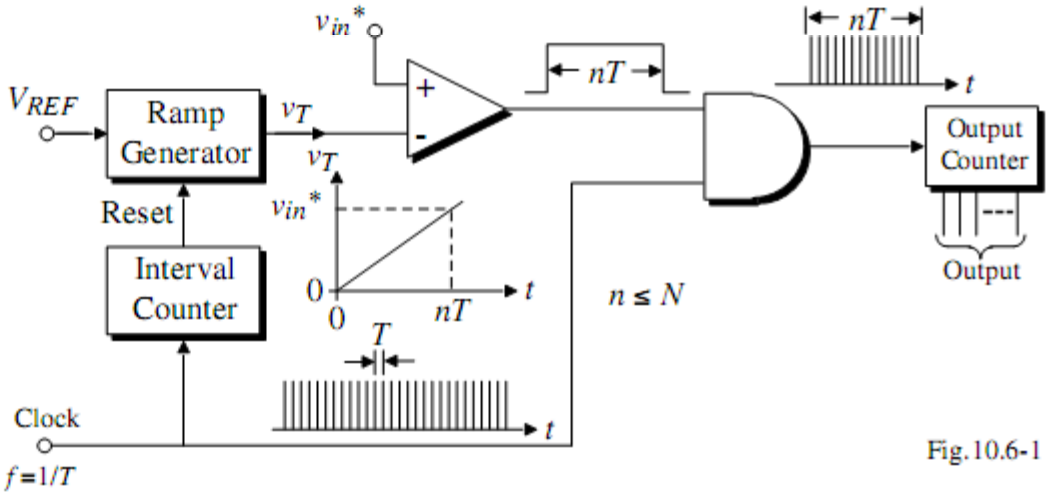


Fig.10.6-1

Attributes:

- Simplicity of operation
- Subject to error in the ramp generator
- Long conversion time ≤ $2^N T$

Dual-slope ADC

Block diagram:

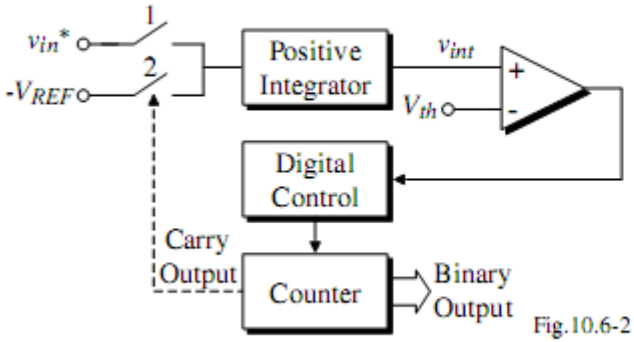


Fig.10.6-2

Waveforms:

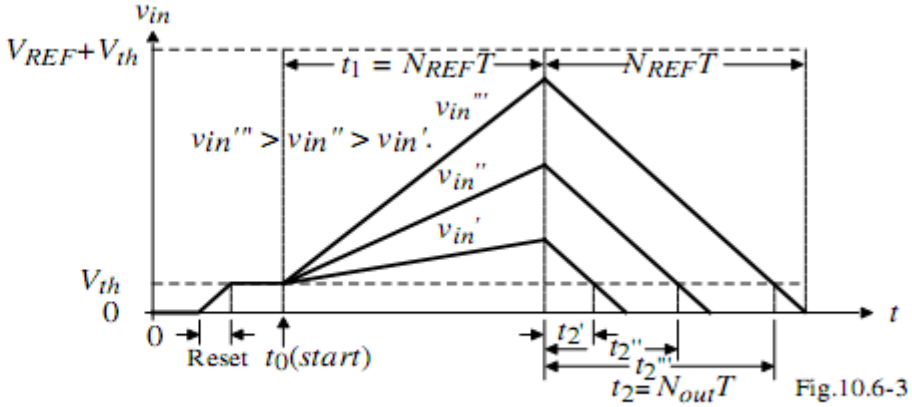


Fig.10.6-3

Operation:

1.) Initially $v_{int} = 0$ and v_{in} is sampled and held ($v_{IN}^* > 0$).

2.) Reset the positive integrator by integrating a positive voltage until $v_{int}(0) = V_{th}$.

3.) Integrate v_{in}^* for N_{REF} clock cycles to get,

$$v_{int}(t_1) = K\int_0^{N_{REF}T} v_{in}^*\,dt + v_{int}(0) = KN_{REF}Tv_{in}^* + V_{th}$$

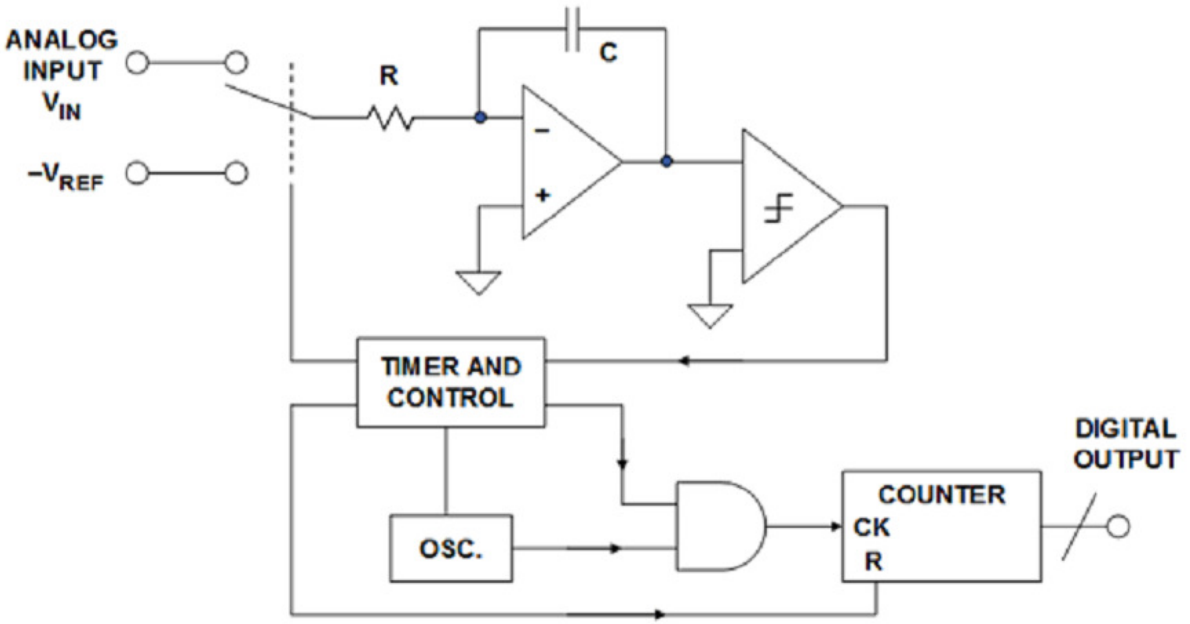
4.) After N_{REF} counts, the carry output of the counter closes switch 2 and-V_{REF} is applied to the positive integrator. The output of the integrator at $t = t_1+t_2$ is,

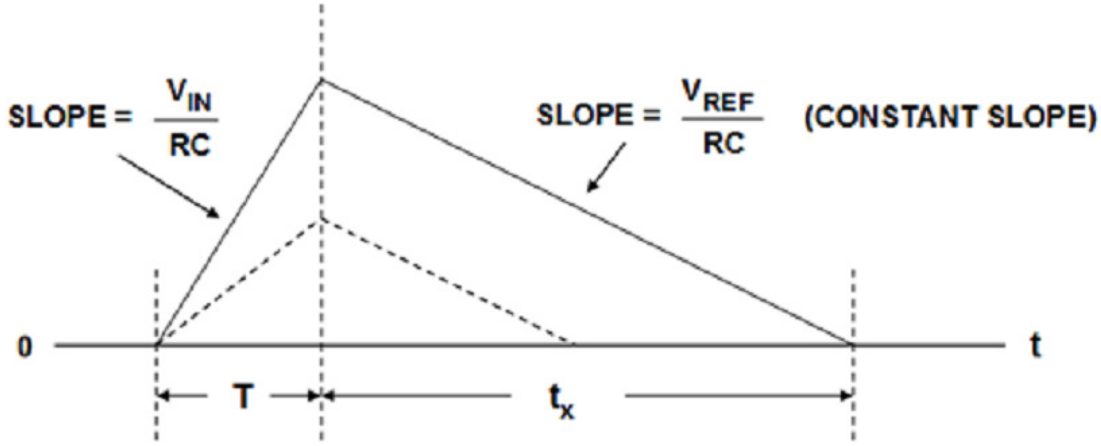
$$v_{int}(t_1+t_2) = v_{int}(t_1)+K\int_{t_1}^{N_{out}T}(-V_{REF})dt = V_{th} \rightarrow KN_{REF}Tv_{in}^*+V_{th} - KN_{out}TV_{REF} = V_{th}$$

5.) Solving for N_{out} gives, $N_{out} = N_{REF}\,(v_{in}^*/V_{REF})$

Comments: Conversion time $\le 2(2^N)T$ and the operation is independent of V_{th} and K.

Dual-slope ADC





$$\frac{V_{IN}}{RC} T = \frac{V_{REF}}{RC} t_x$$

$$t_x = \frac{V_{IN}}{V_{REF}} T$$

Successive approximation algorithm

Successive Approximation Algorithm:

1.) Start with the *MSB* bit and work toward the *LSB* bit.

2.) Guess the *MSB* bit as 1.

3.) Apply the digital word 10000.... to a DAC.

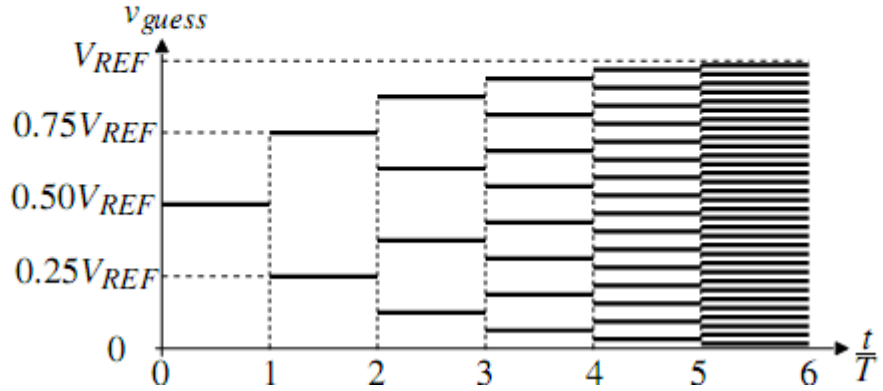
4.) Compare the DAC output with the sampled analog input voltage.

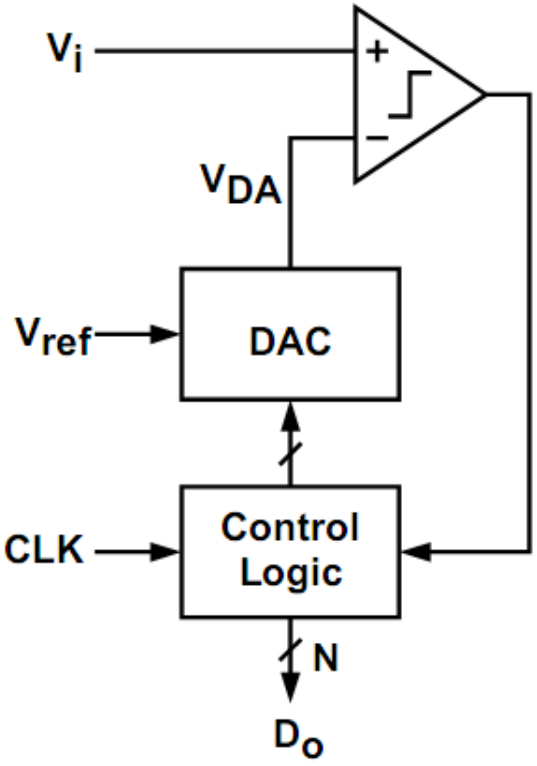
5.) If the DAC output is greater, keep the guess of 1. If the DAC output is less, change the guess to 0.

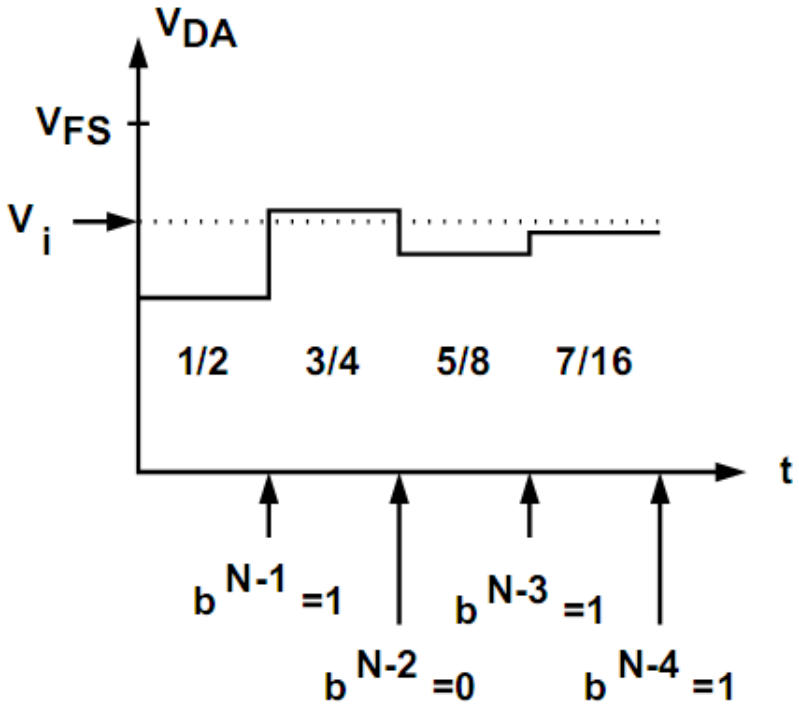
6.) Repeat for the next *MSB*.

If the number of bits is N, the time for conversion will be NT where T is the clock period.

Illustration:







Successive Approximation ADC

- Binary search of possible subregions.
- Fraction of VFS corresponding to each bit is successively (starting with MSB) added to fraction corresponding to already determined bits and sum is compared to input.
- N comparisons per conversion.
- Requires a high-speed DAC with precision on the order of the converter itself.
- Excellent trade-off between accuracy and speed.

5-bit SA ADC

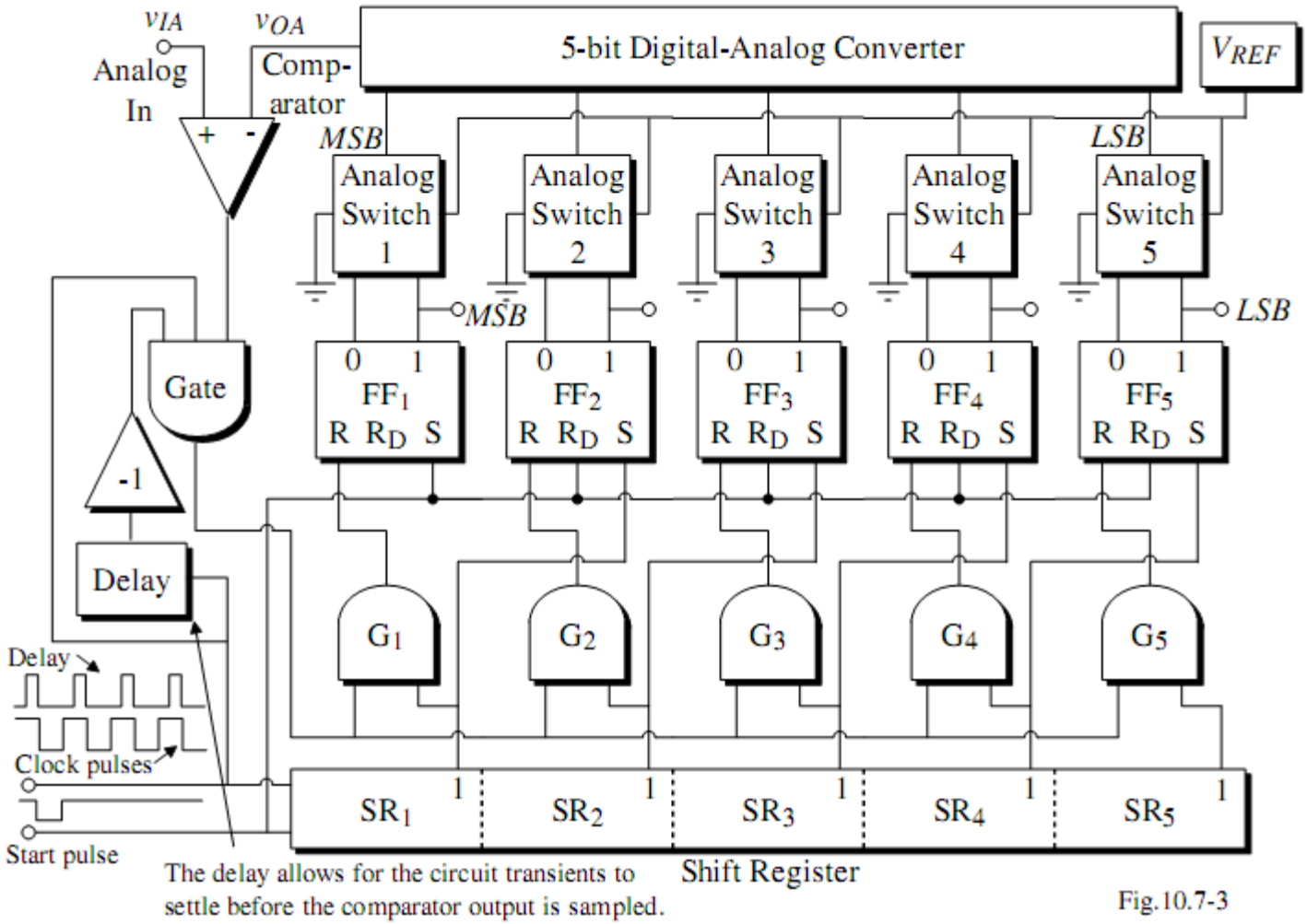
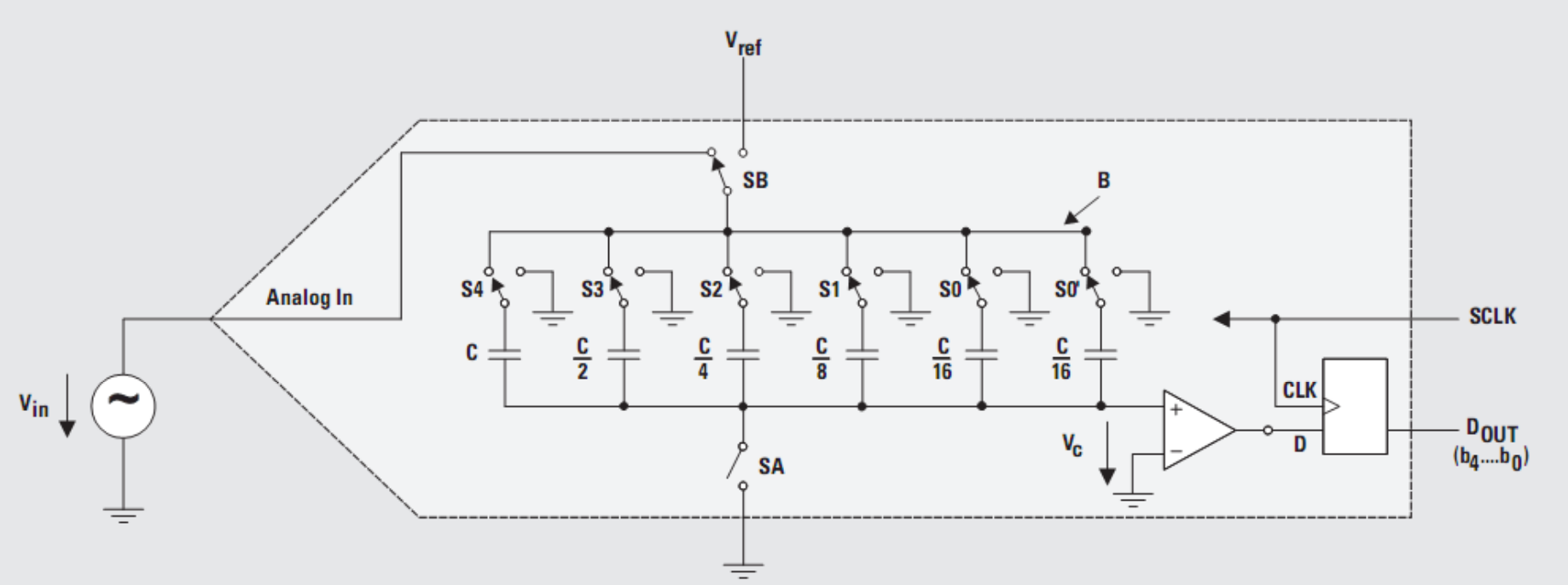


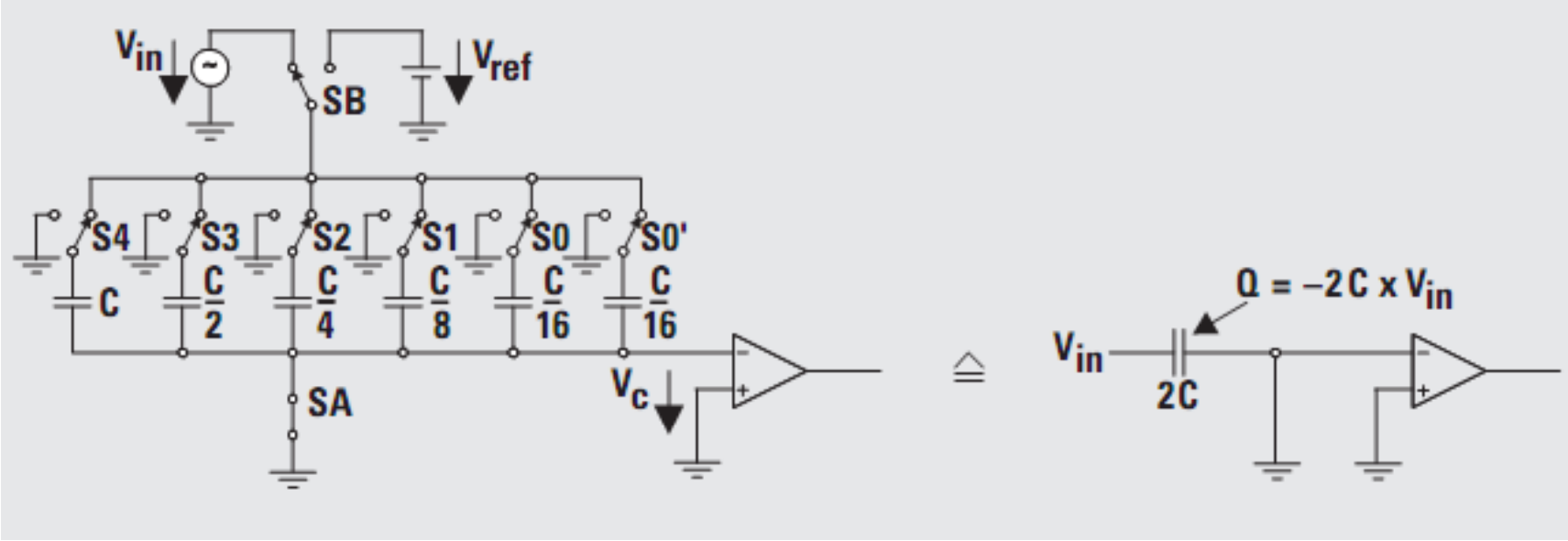
Fig.10.7-3

SAR ADC based on charge redistribution (5-bit example)



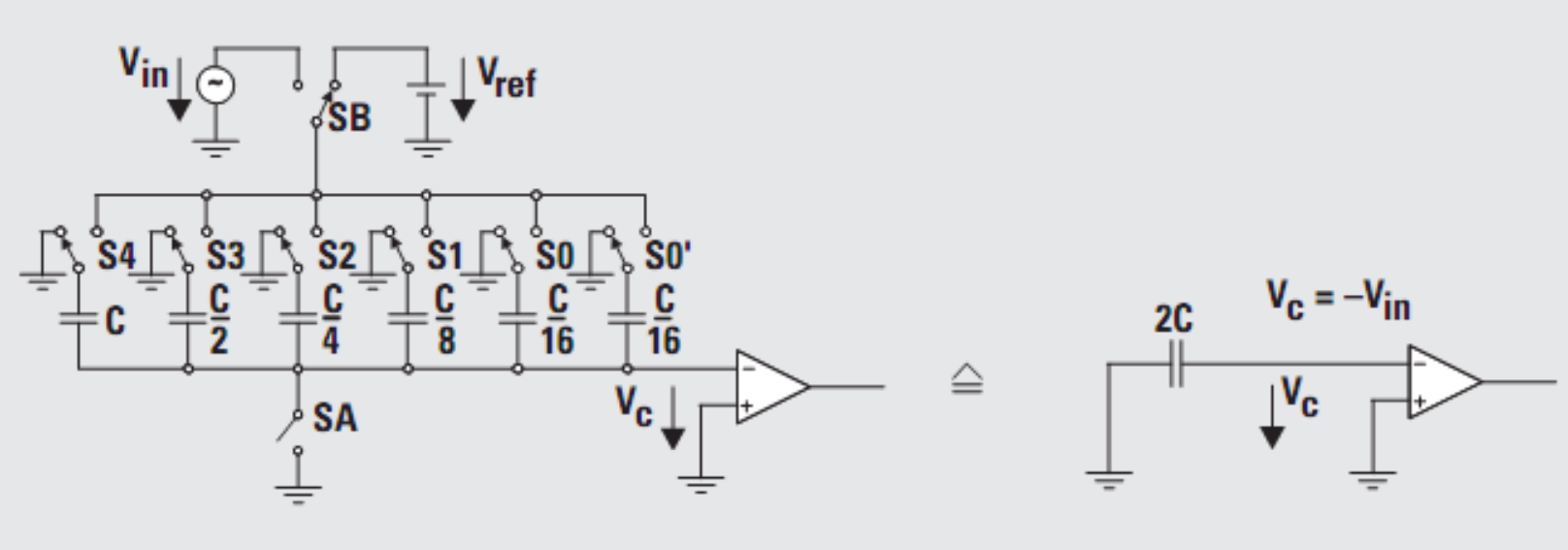
- All capacitors have binary weighted values, i.e., C, C/2, C/4,….C/2n–1. The last two capacitors having the value C/2n–1 are connected so that the total capacitance of the n+1 capacitors is 2C. MOS-transistors are used to implement the required n+3 switches, and the voltage comparator provides the appropriate steering of the switches via auxiliary logic circuitry. The conversion process is performed in three steps: the sample mode, the hold mode, and the redistribution mode (in which the actual conversion is performed).

SAR ADC based on charge redistribution: Sample-mode



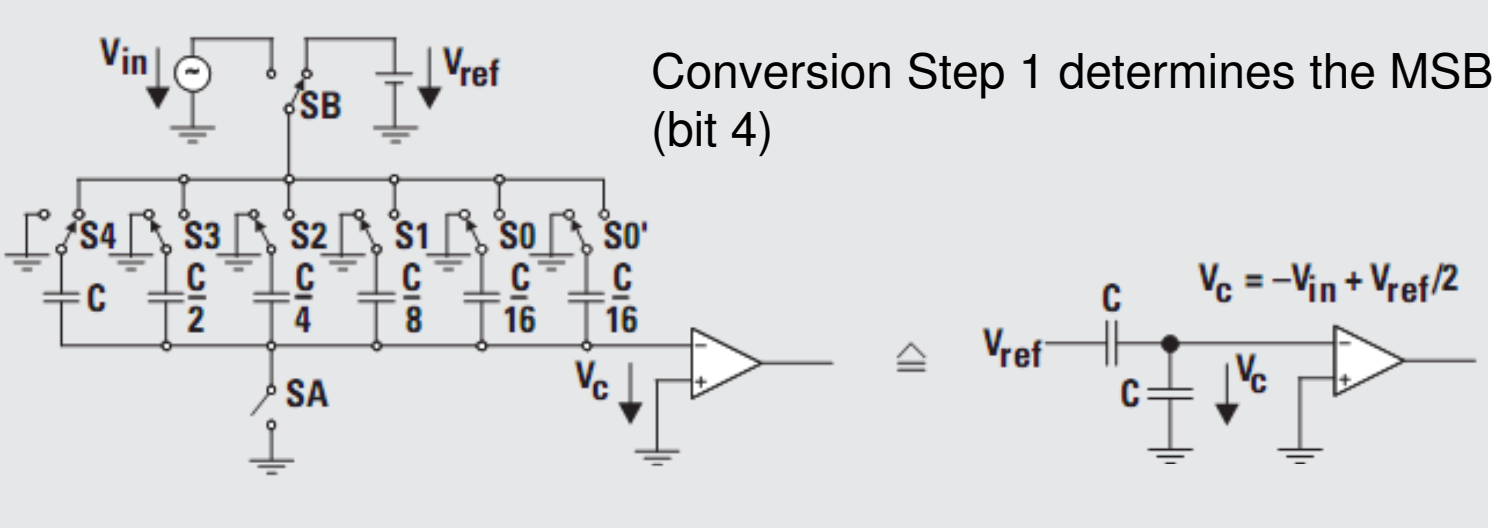
- Sample mode
- In the sampling mode, switch SA is closed and SB is switched to the input voltage Vin. The remaining switches are turned to the common bus B. Due to charging, a total charge of Qin = –2C x Vin is stored on the lower plates of the capacitors

SAR ADC based on charge redistribution: Hold-mode



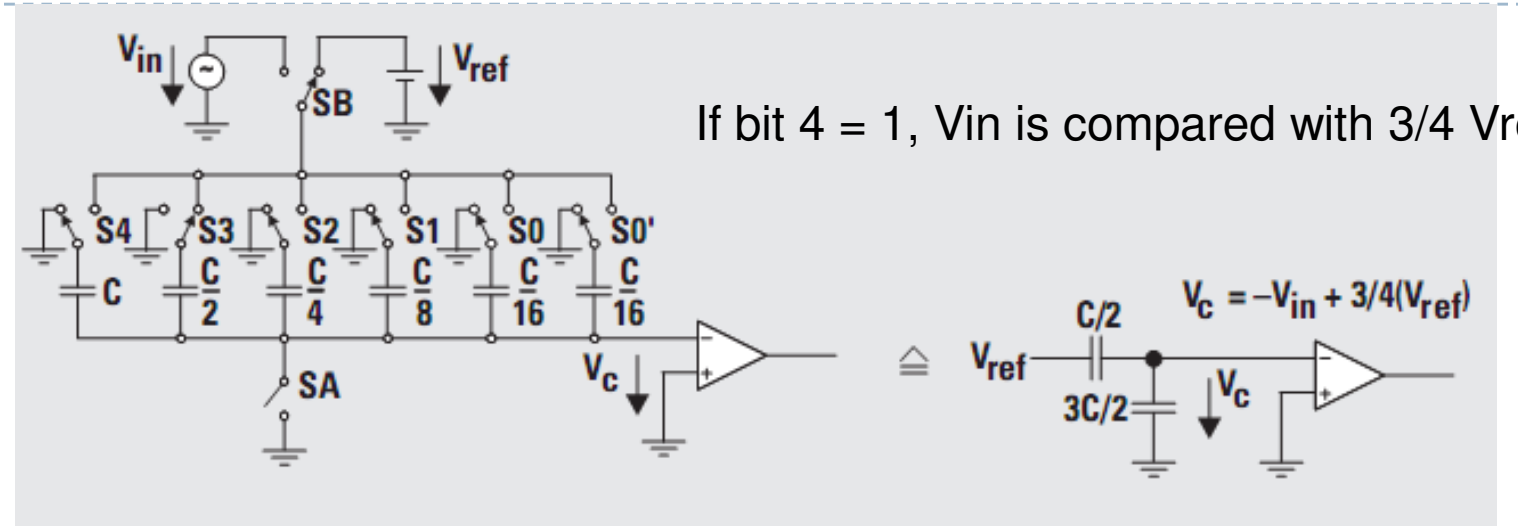
- Hold mode
- During the hold mode (Figure 3), switch SA is opened while the switches S4….S0′ are connected to ground thereby applying a voltage of V c = –Vin to the comparator input. This means that the circuit already has a built-in sample-and-hold element.

SAR ADC based on charge redistribution: redistribution mode



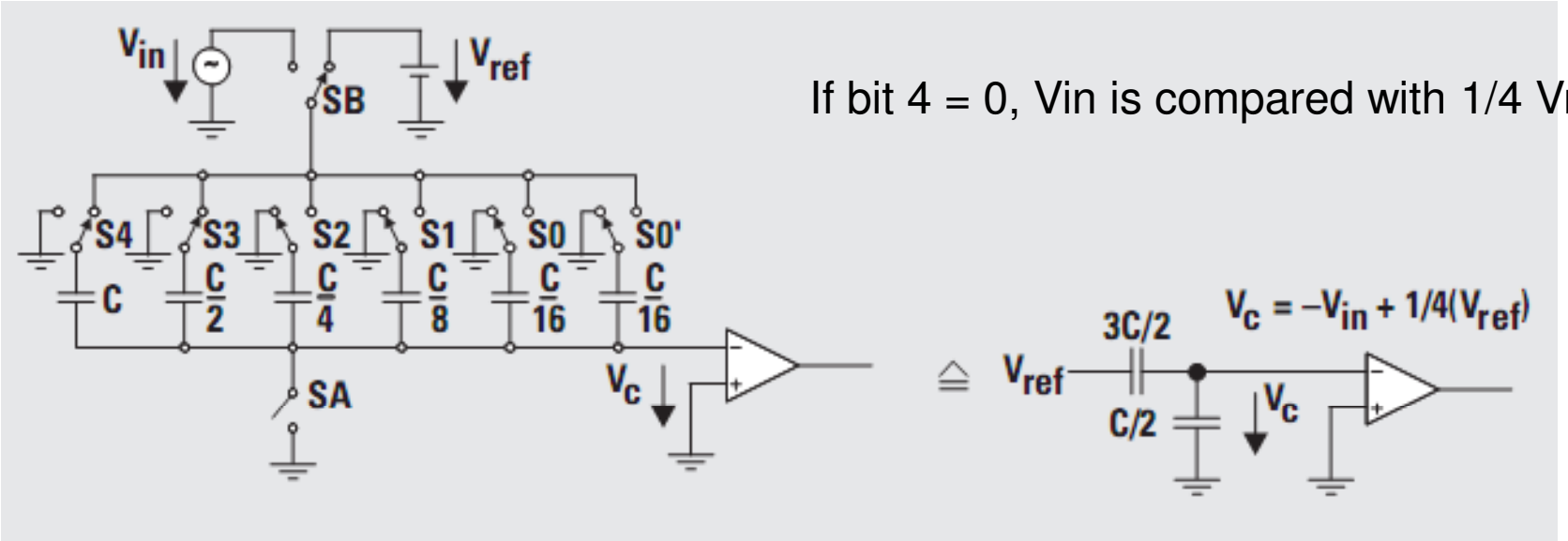
- The actual conversion is performed by the redistribution mode. The first con-
- version step connects C (the largest capacitor) via switch S4 to the reference voltage Vref, which corresponds to the full-scale range (FSR) of the ADC. Capacitor C forms a 1:1 capacitance divider with the remaining capacitors connected to ground. The comparator input voltage becomes V c = –Vin + Vref /2.
- If Vin > Vref /2, then V c < 0, and the comparator output goes high, providing the most significant bit MSB (bit 4) = 1. On the other hand, if Vin < Vref /2, then V c > 0, and bit 4 = 0

SAR ADC based on charge redistribution: redistribution mode



- The second conversion step connects C/2 to Vref . If the first conversion step resulted in bit 4 = 1, switch S4 is turned to ground again to discharge C; otherwise it remains connected to Vref if bit 4 = 0, resulting in a comparator input voltage V c = Vin + bit 4 – Vref /2 + Vref /4.
- According to this voltage, the next most significant bit (bit 3) is obtained by comparing Vin to 1/4 Vref or 3/4 Vref through the different voltage dividers. Switch S3 is then either turned to ground if bit 3 = 1, thereby discharging C/2, or S3 remains connected to Vref if bit 3 = 0.

SAR ADC based on charge redistribution: redistribution mode



- This process continues until all bits are generated, with the final conversion step being performed at a comparator input voltage of V c = –Vin + bit 4 x Vref /2 + bit 3 x Vref /4 + bit 2 x Vref /8 + bit 1 x Vref /16 + bit 0 x Vref /32.

Flash ADC

A 3-bit, parallel ADC:

Comments:

- Fast, in the first phase of the clock the analog input is sampled and applied to the comparators. In the second phase, the digital encoding network determines the correct output digital word.
- Number of comparator required is 2^N-1
- Can put a sample-hold at the input or can used clocked comparators
- Typical sampling frequencies can be as high as 400MHz for 6-bits in sub-micron CMOS technology.

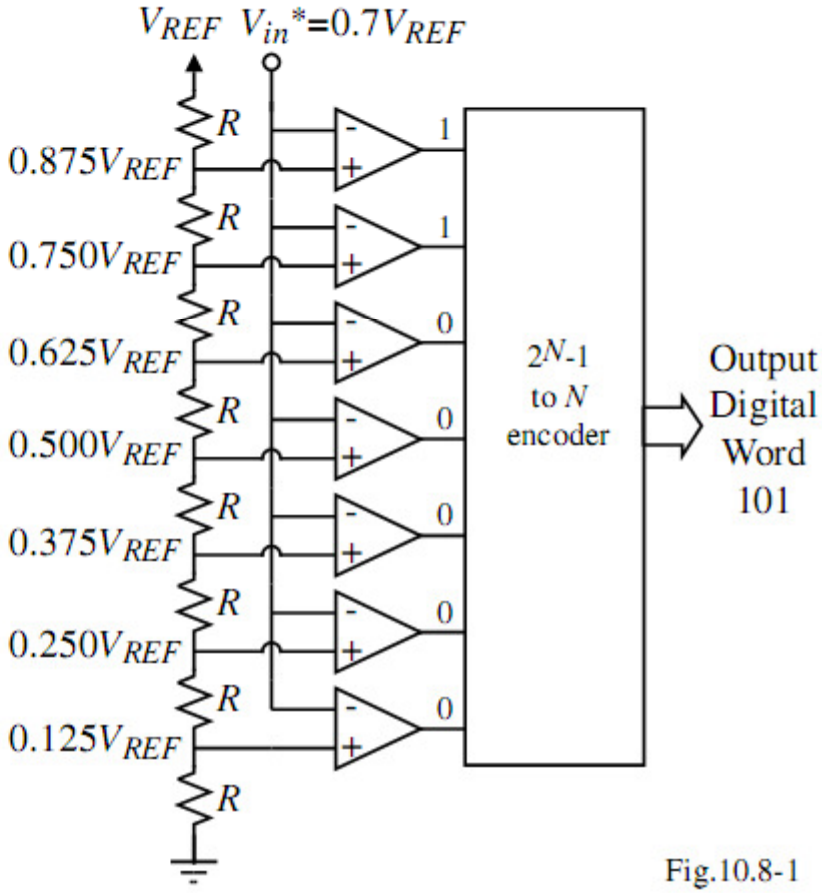
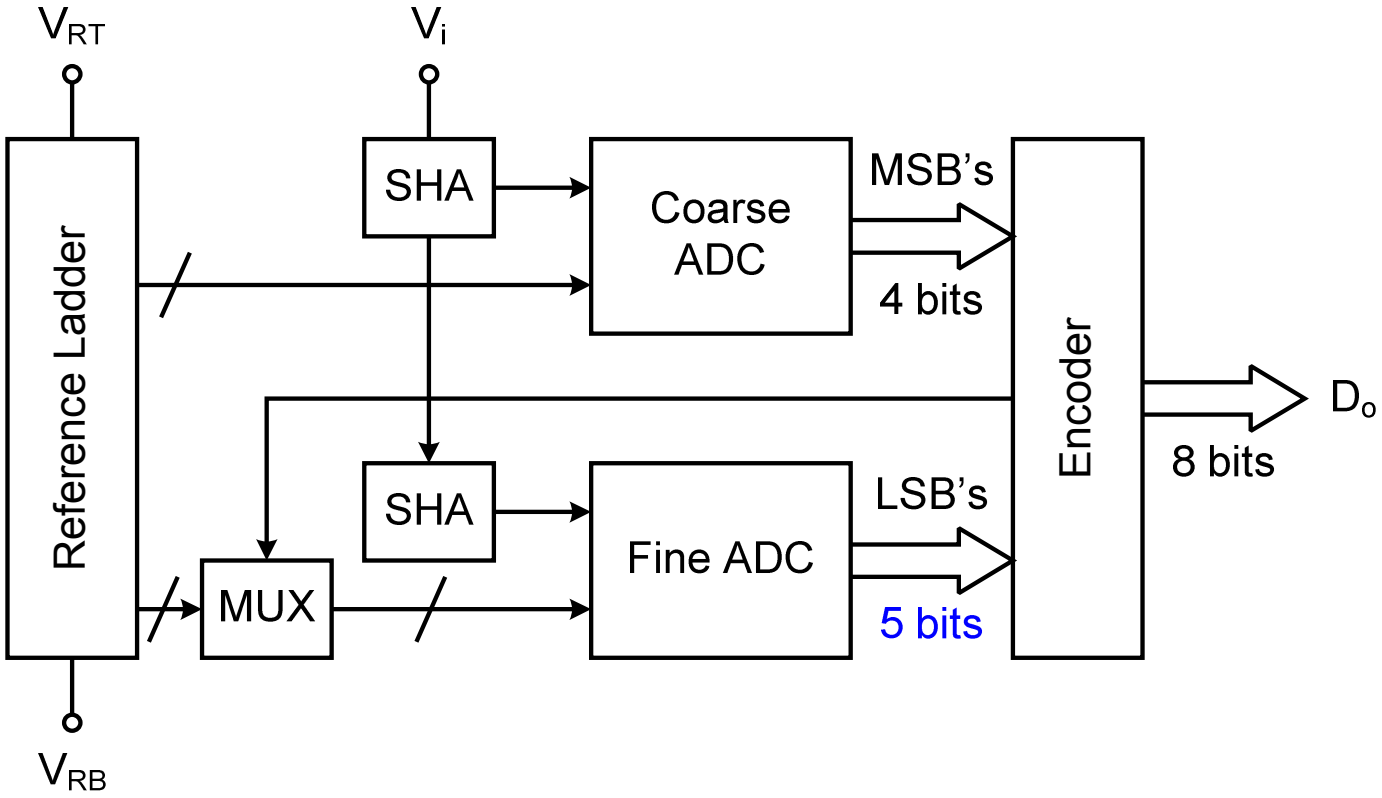


Fig.10.8-1

Subranging ADC

- Reduce the number of comparators



Interpolating ADC

A 3-bit interpolating ADC using a factor of 4 interpolation:

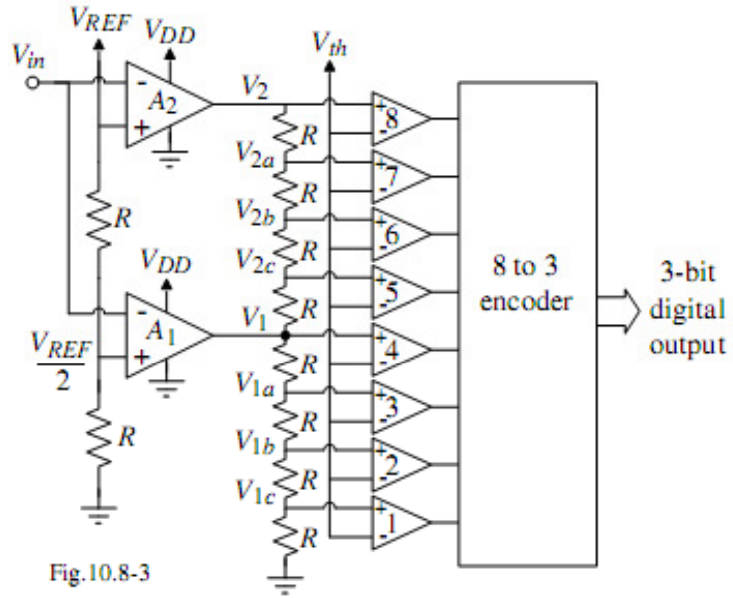


Fig.10.8-3

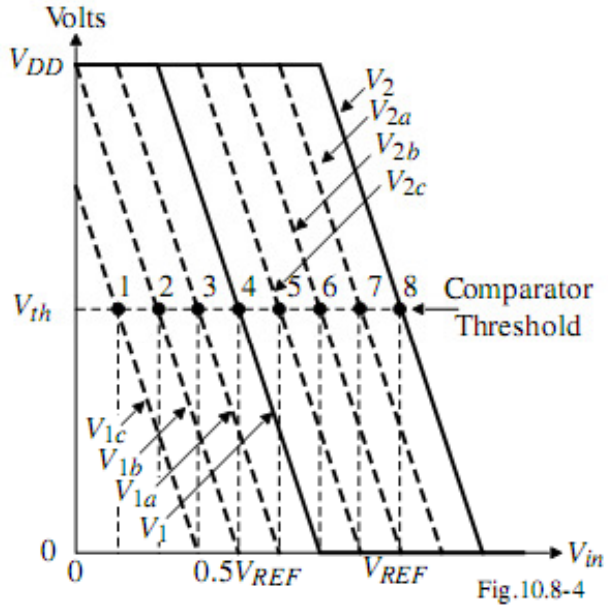


Fig.10.8-4

Comments:

- Loading of the input is reduced from 8 comparators to two amplifiers.
- The comparators no longer need a large *ICMR*
- V_1 and V_2, are interpolated through the resistor string and applied to the comparators.
- Because of the amplification of the input amplifiers and a single threshold, the comparators can be simple and are often replaced by a latch.

Folding ADC

- Reduce the number of comparators

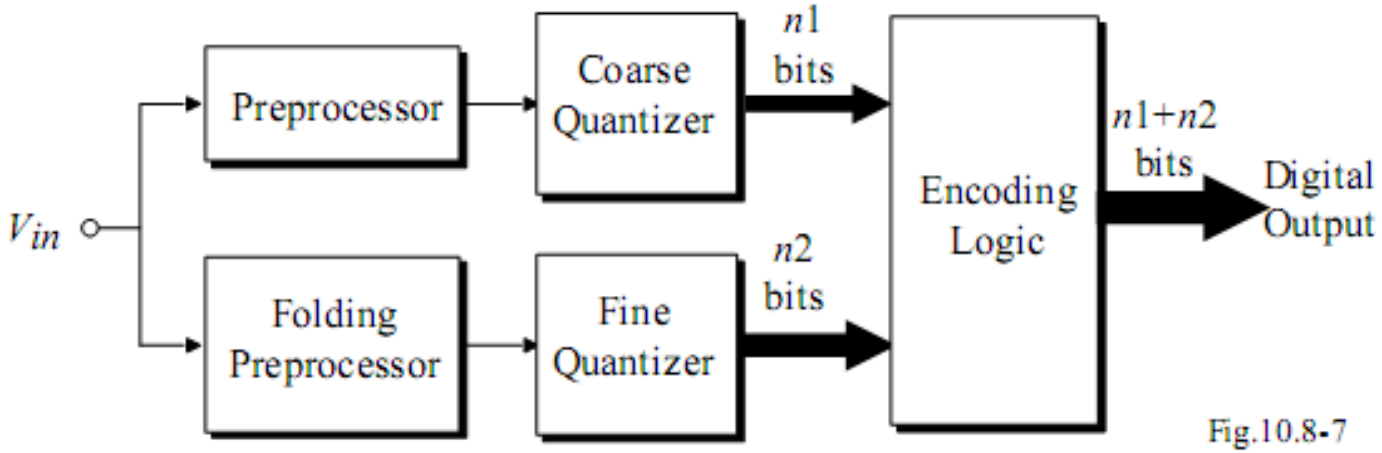


Fig.10.8-7

- The input is split into two or more parallel paths.
  - First path uses a coarse quantizer to quantize the signal into 2n1 values
  - The second path maps all of the 2^{n1} subranges onto a single subrange and applies this analog signal to a fine quantizer of 2^{n2} subranges.
- Thus, the total number of comparators is $2^{n1}-1 + 2^{n2}-1$ compared with $2^{n1+n2}-1$ for a parallel ADC. i.e., if n1 = 2 and n2 = 4, the folding ADC requires 3 + 15 = 18 compared with 63 comparators.

Folding ADC

Folding characteristic for $n1 = 2$ and $n2 = 3$.

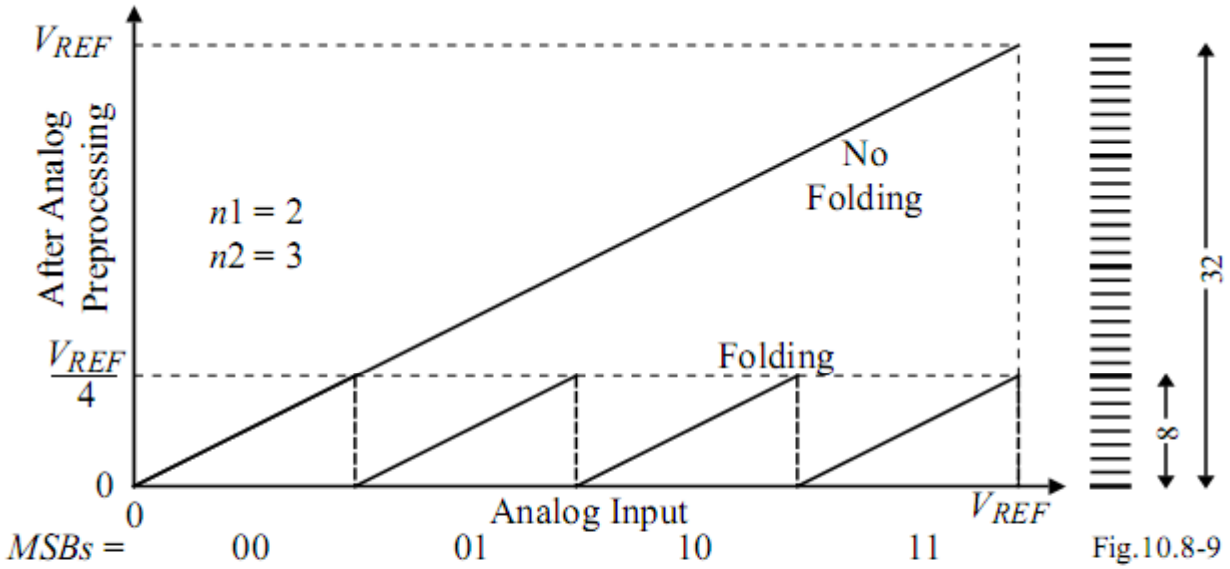
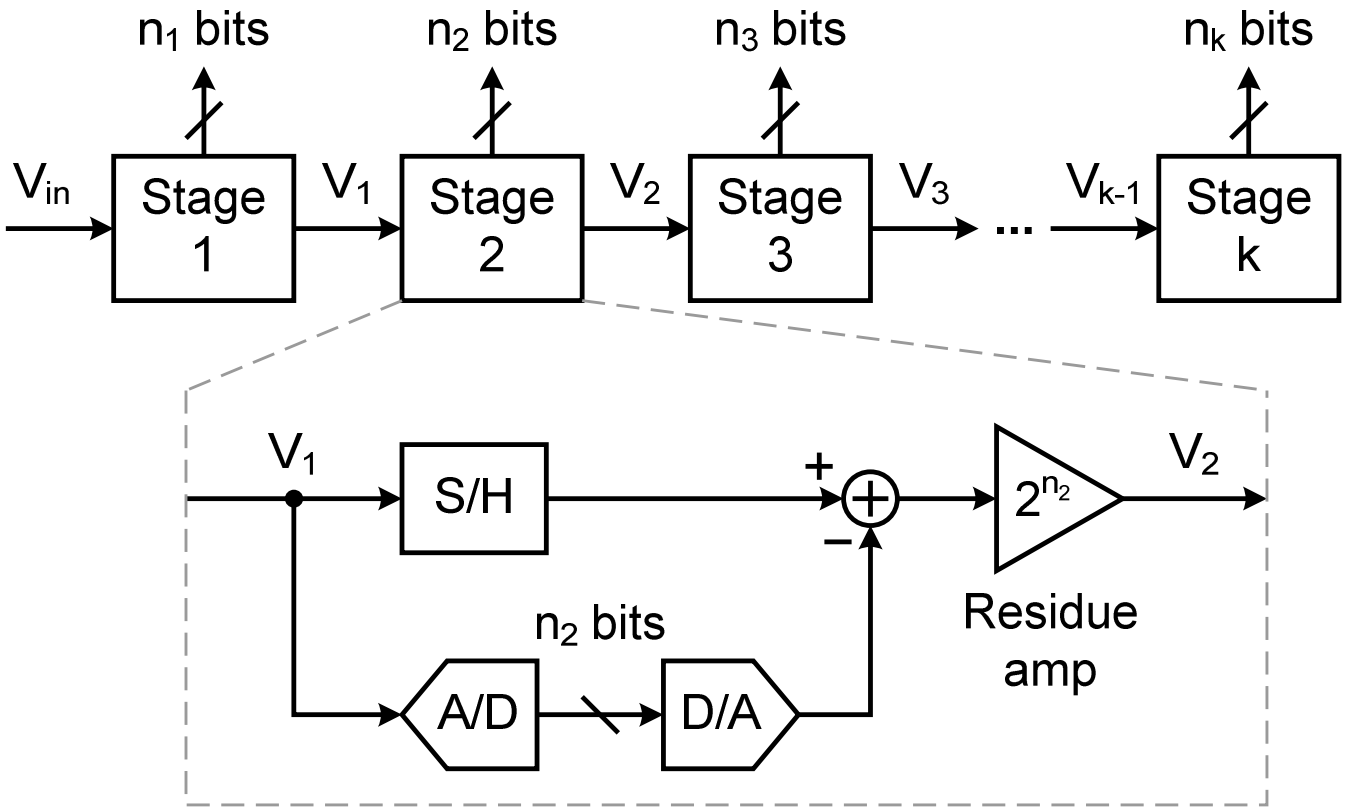


Fig.10.8-9

Problems:

- The sharp discontinuities of the folder are difficult to implement at high speeds.
- Fine quantizer must work at voltages ranging from 0 to $V_{REF}/4$ (subranging).
- The actual frequency of the folding signal is F times the input frequency where F is the number of folds

Pipelined ADC



Operation of pipelined ADC