CMOS operational amplfier

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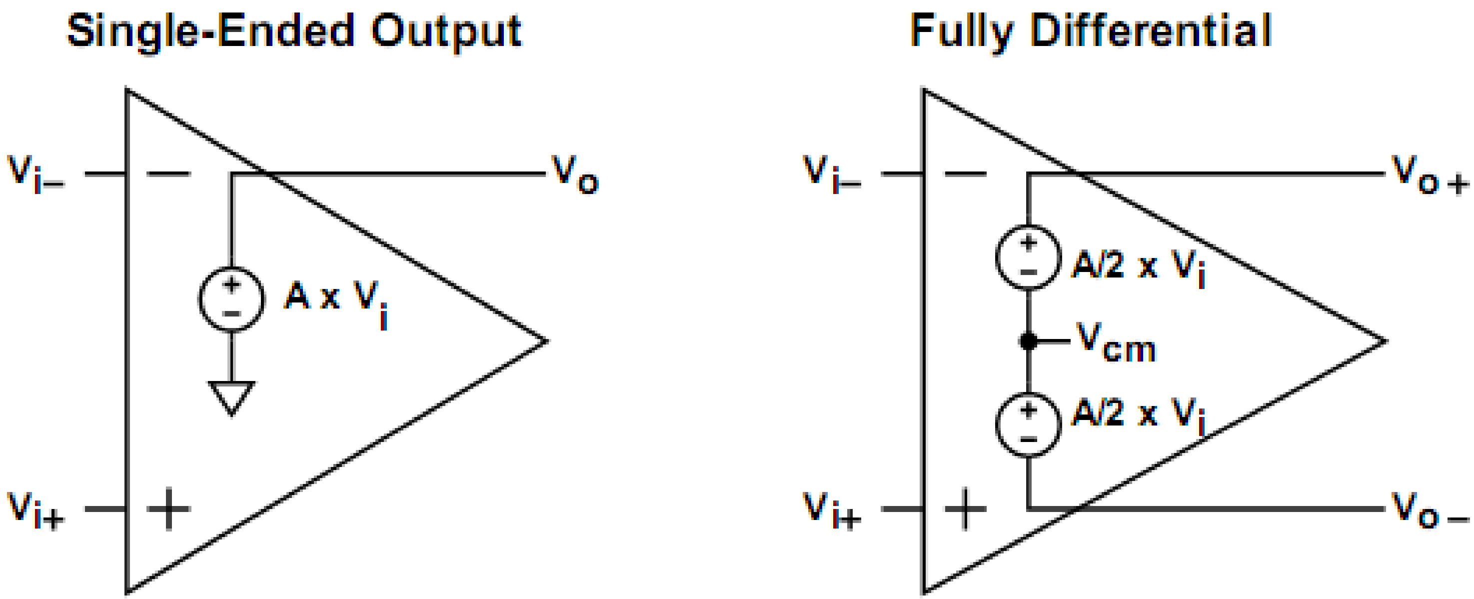
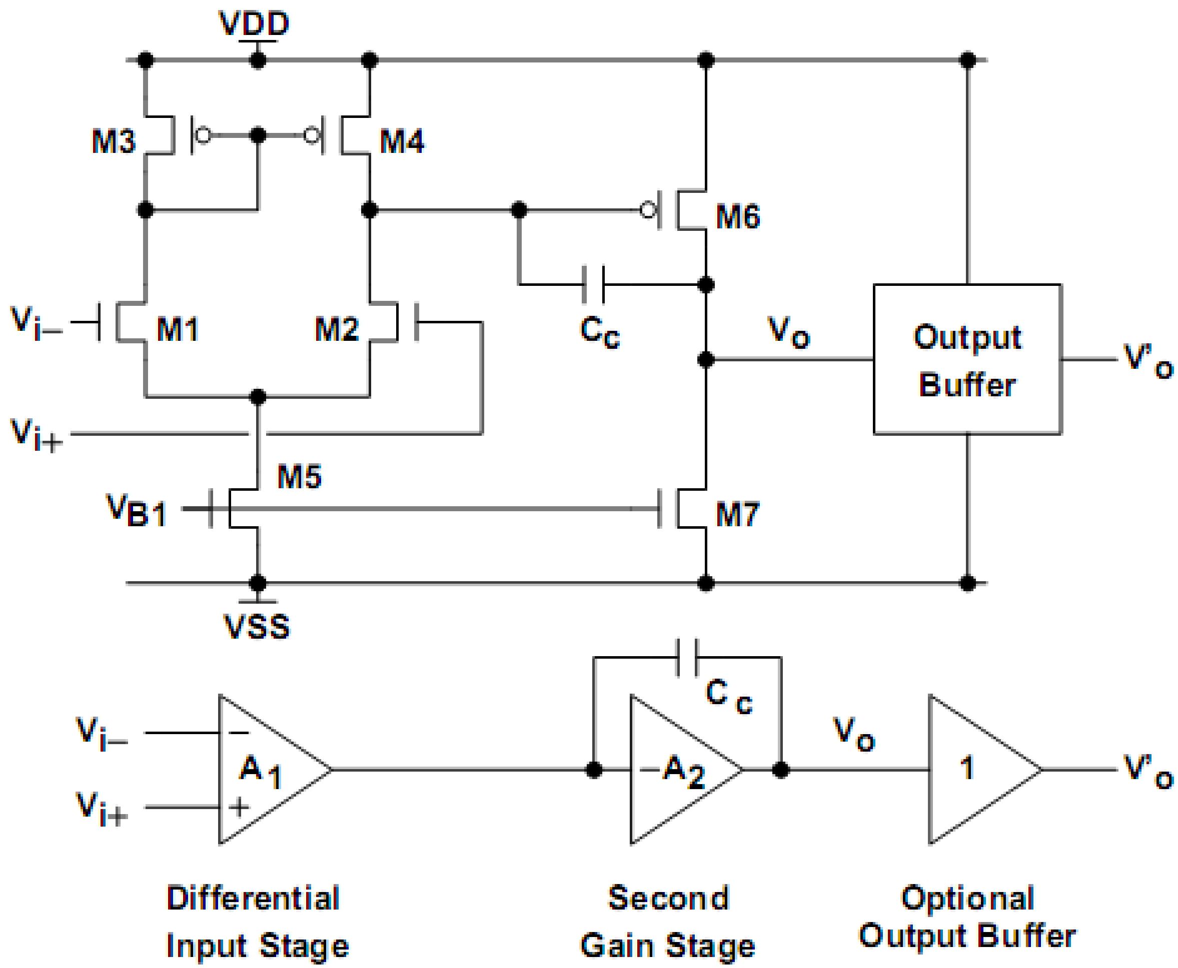
Ideal opamp

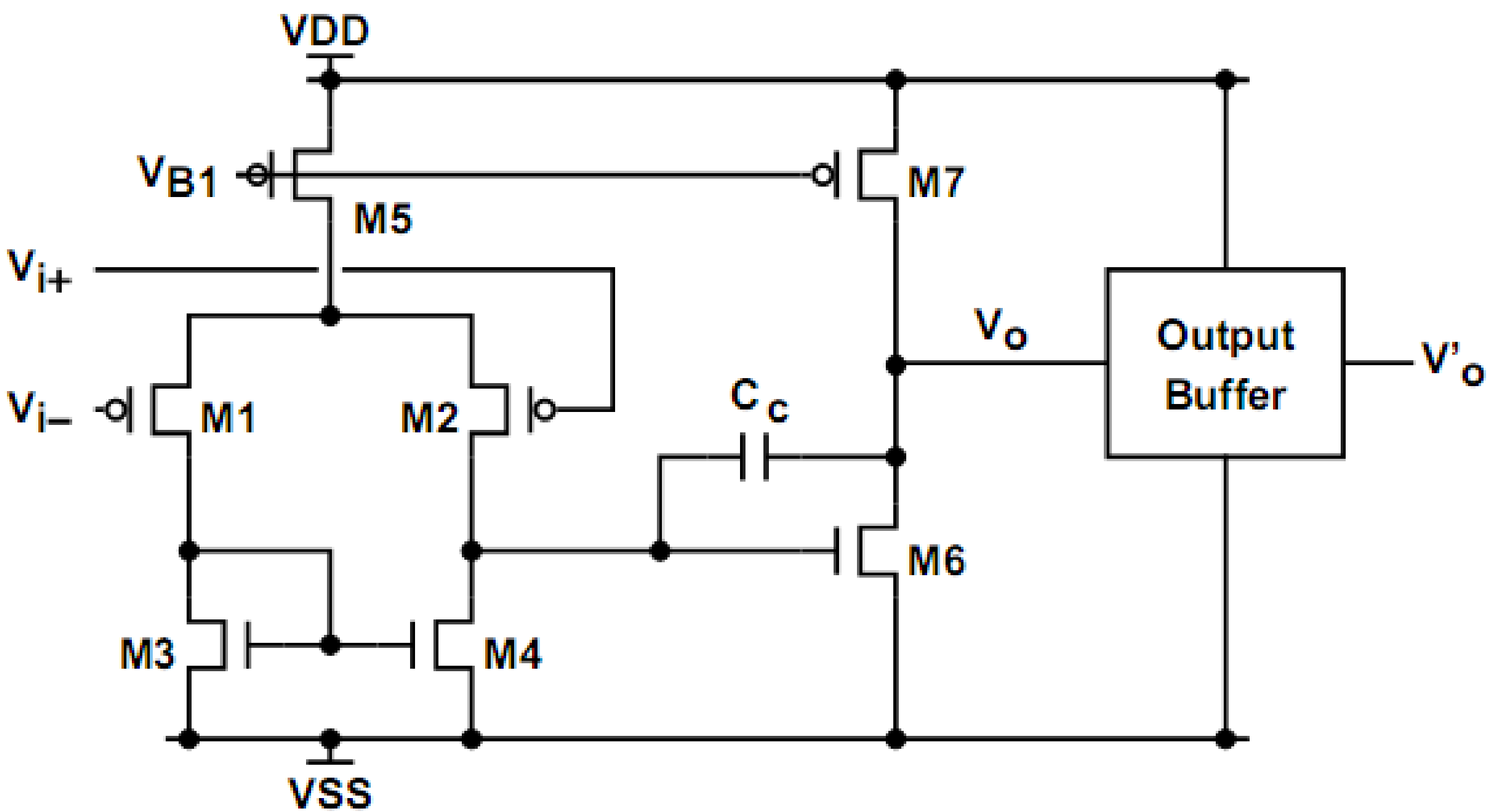


- $V_o = A \times V_i$
- Ideal opamp:
  - $A \rightarrow \infty$, $Z_{in} \rightarrow \infty$, $Z_{out} \rightarrow 0$.
  - No frequency dependence.

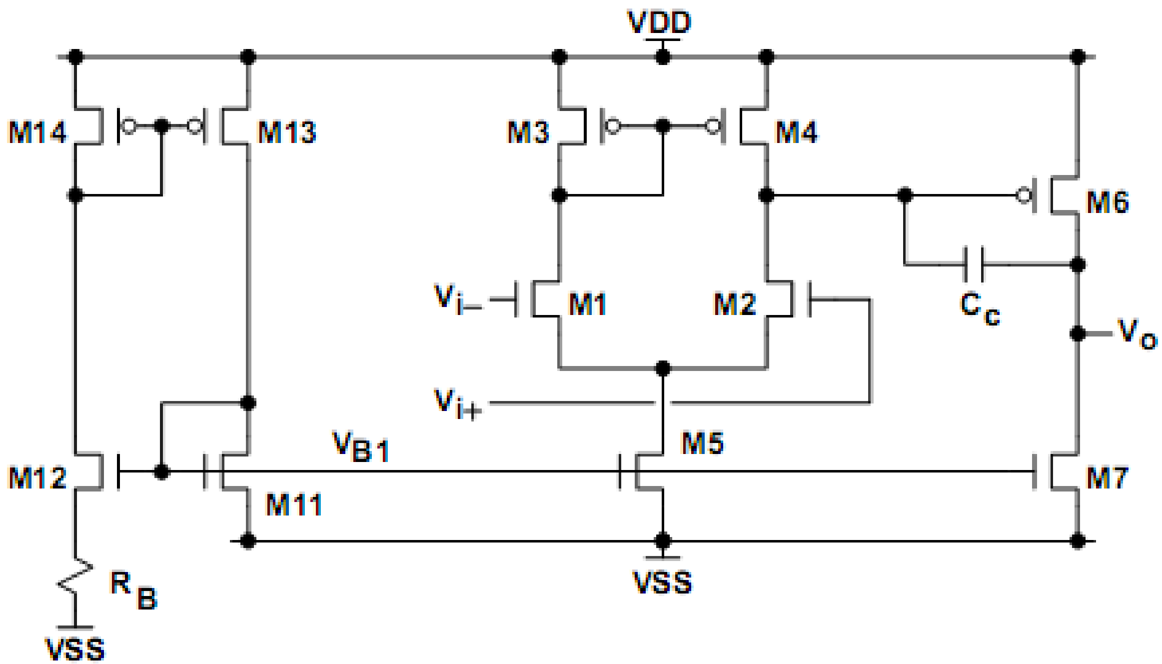
Basic 2-stage opamp



PMOS input 2-stage opamp



Constant gm bias generator



$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$$

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4$$

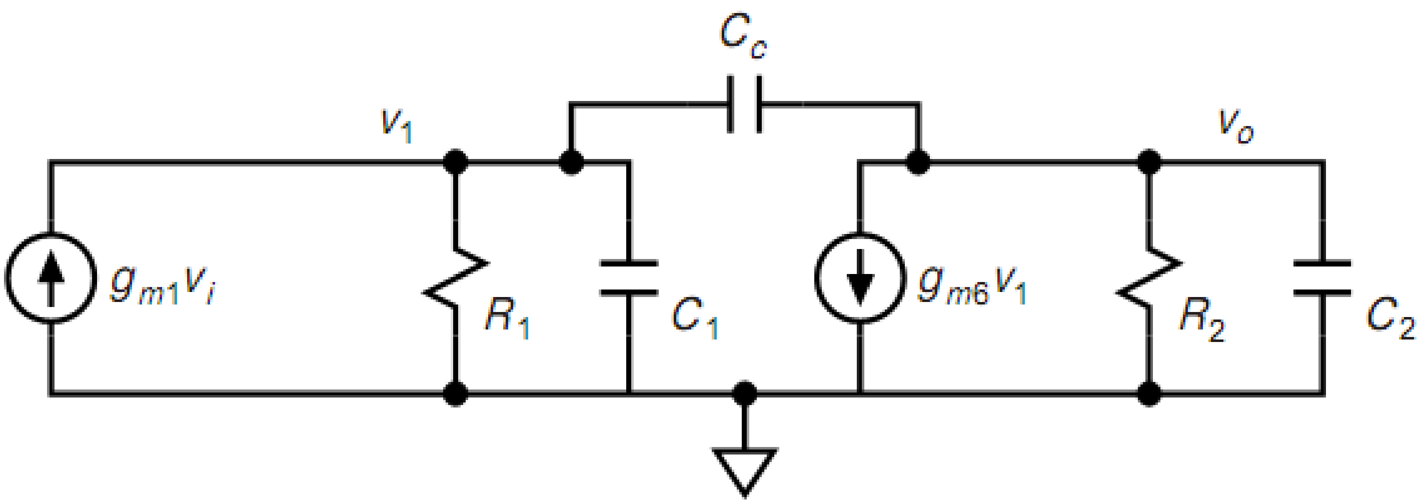
$$\left(\frac{W}{L}\right)_{13} = \left(\frac{W}{L}\right)_{14}$$

$$\left(\frac{W}{L}\right)_{12} = \alpha \cdot \left(\frac{W}{L}\right)_{11}$$

$$g_m = \sqrt{2\mu C_{ox}(W/L)I_D} \quad g_{m11} = \frac{2}{R_B}\frac{\sqrt{\alpha}-1}{\sqrt{\alpha}} \quad g_{m1,m2} = g_{m11} \cdot \sqrt{\frac{(W/L)_1}{(W/L)_{11}}}\sqrt{\frac{1}{2}\frac{(W/L)_5}{(W/L)_{11}}}$$

$$g_{m3,m4} = g_{m11} \cdot \sqrt{\frac{\mu_p}{\mu_n}}\sqrt{\frac{(W/L)_3}{(W/L)_{11}}}\sqrt{\frac{1}{2}\frac{(W/L)_5}{(W/L)_{11}}} \quad g_{m6} = g_{m11} \cdot \sqrt{\frac{\mu_p}{\mu_n}}\sqrt{\frac{(W/L)_6}{(W/L)_{11}}}\sqrt{\frac{(W/L)_7}{(W/L)_{11}}}$$

Simplified 2-stage model



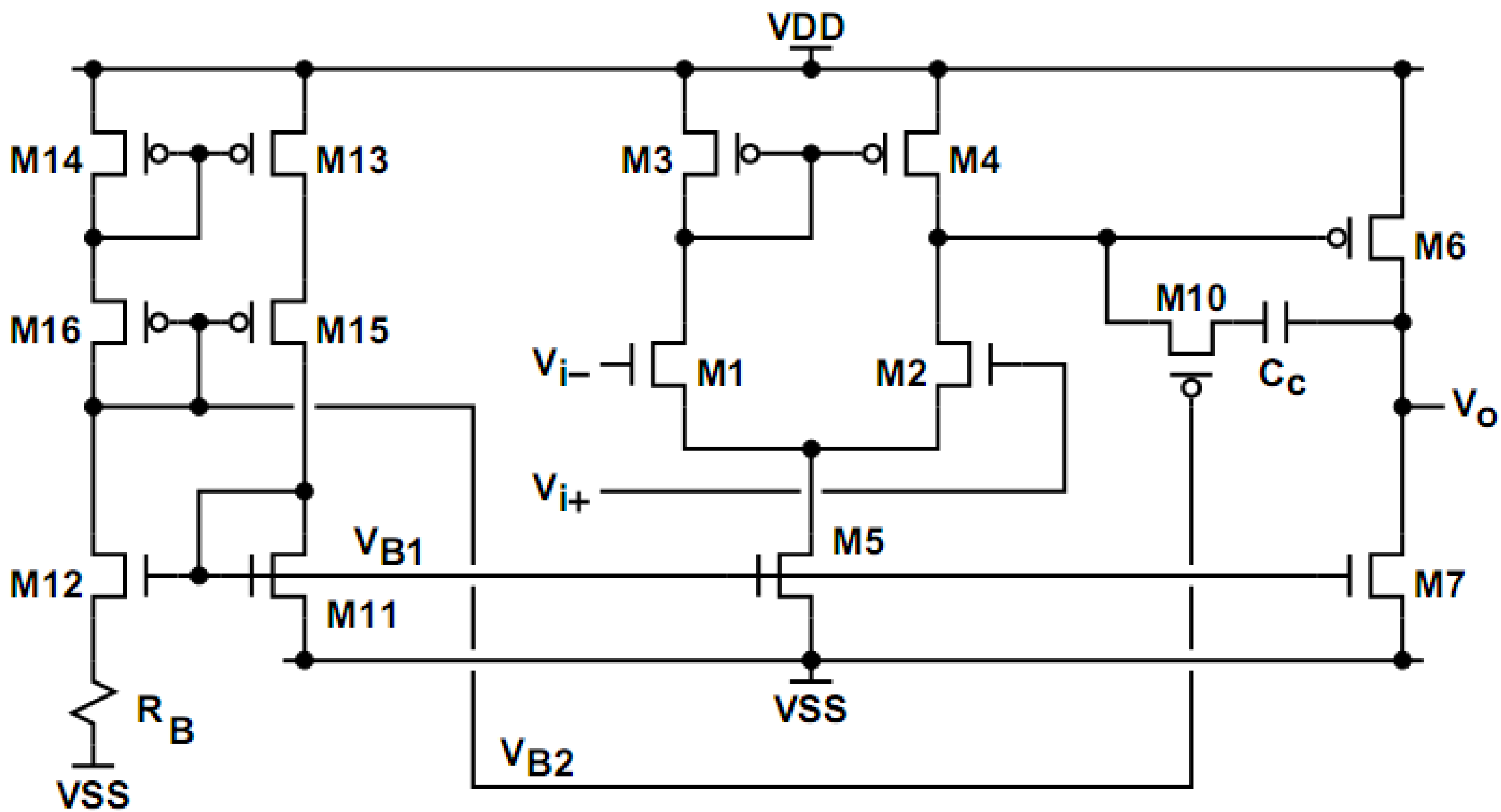
$$G_1 = g_{o2} + g_{o4} \qquad G_2 = g_{o6} + g_{o7} \qquad C_1 \simeq C_{gs6}$$

$$A_v \equiv \frac{v_o}{v_i} = A_v(0)\frac{1 - s/z_1}{(1 - s/p_1)(1 - s/p_2)}$$

$$A_v(0) = g_{m1}g_{m6}R_1R_2$$

$$p_1 \approx -\frac{g_{m1}}{C_c} \times \frac{1}{A_v(0)} \qquad p_2 \approx -\frac{g_{m6}}{C_1 + C_2} \qquad z_1 = +\frac{g_{m6}}{C_c}$$

Frequency compensation using nulling resistor



Frequency compensation using nulling resistor

- The zero-nulling resistor R_c is realized by M10 in the triode region.

$$z_1 = \frac{1}{(1/g_{m6} - R_c)C_c} = -\frac{g_{m6}}{(g_{m6}R_c - 1)C_c}$$

- Let $\frac{(W/L)_{13}}{(W/L)_{14}} = \frac{(W/L)_{15}}{(W/L)_{16}}$ and $\frac{(W/L)_7}{(W/L)_{11}} = \frac{(W/L)_6}{(W/L)_{13}}$, then

$$V_{ov6} = V_{ov13} = V_{ov14} \qquad V_{ov10} = V_{ov15} = V_{ov16} \qquad \frac{V_{ov6}}{V_{ov10}} = \frac{V_{ov13}}{V_{ov15}} = \sqrt{\frac{(W/L)_{15}}{(W/L)_{13}}}$$

$$g_{m6}R_c = \frac{g_{m6}}{g_{m10}} = \frac{(W/L)_6}{(W/L)_{10}}\frac{V_{ov6}}{V_{ov10}} = \frac{(W/L)_6}{(W/L)_{10}}\sqrt{\frac{(W/L)_{15}}{(W/L)_{13}}}$$

- $p_2/z_1 \approx (g_{m6}R_c - 1)C_c/(C_1 + C_2)$ is independent of process and temperature variations.

Voltage and current range

Input Common-Mode Range

$$V_{ic(max)} = V_{DD} - V_{GS3} + V_{t1} \qquad V_{ic(min)} = V_{SS} + V_{DSAT5} + V_{GS1}$$

- The range is limited to the voltage levels where any transistor goes out of saturation.

Output Voltage Range

$$V_{o(max)} = V_{DD} - V_{DSAT6} \qquad V_{o(min)} = V_{SS} + V_{DSAT7}$$

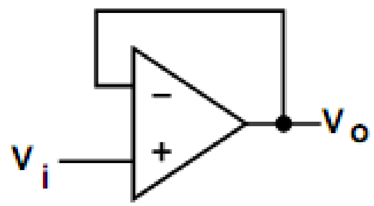
- Output resistive load can also limit the voltage range, if the available output current is insufficient.

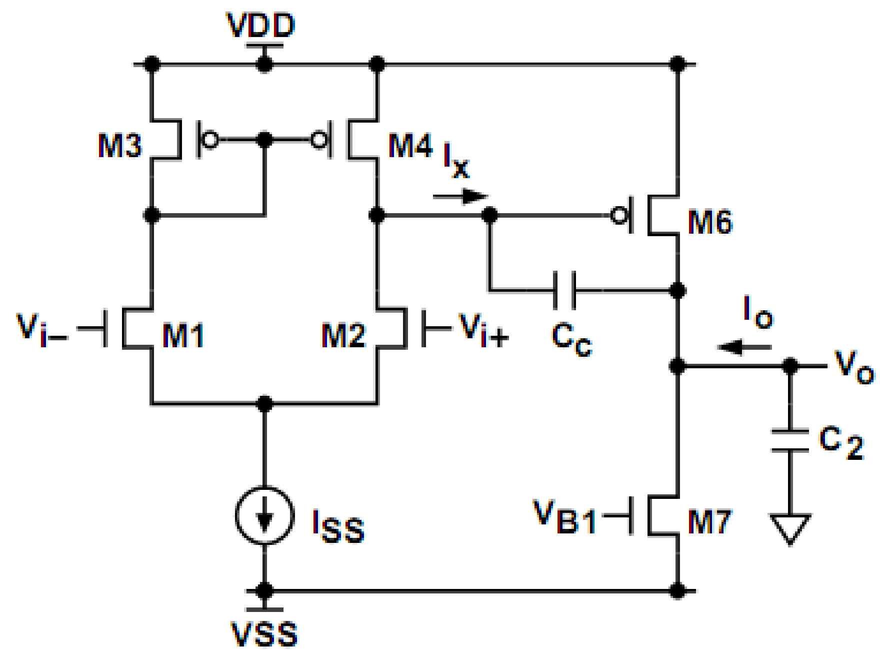
Maximum Output Current

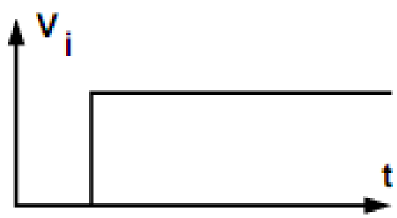
$$I_{o(\text{sink,max})} = I_{D7} \qquad I_{o(\text{source,max})} = \frac{1}{2}k'_p\left(\frac{W}{L}\right)_6[V_{gs6(max)} - V_{t6}]^2 - I_{D7}$$

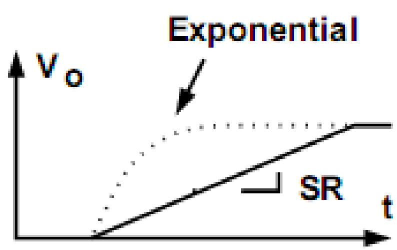
$$V_{gs6(max)} = V_{DD} - V_{i+} + V_{t2}$$

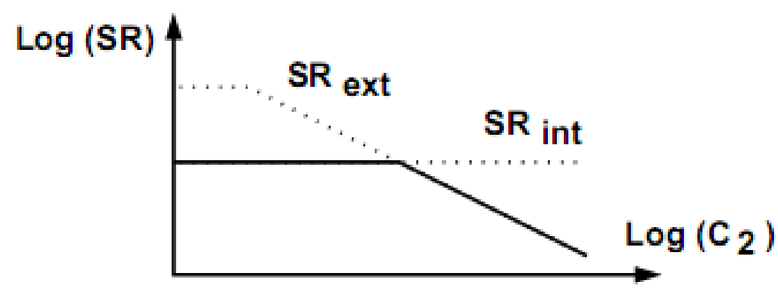
Slew rate


–
+
V i
V o


VDD
M3
M4
I x
M6
V i–
M1
M2
V i+
C C
I o
V o
C 2
I SS
V B1
M7
VSS


V i
t


Exponential
V o
SR
t


Log (SR)
SR ext
SR int
Log (C 2)

Slew rate

The *internal slew rate* is generally limited by current available to charge and discharge C_c from input stage. Therefore,

$$
\begin{aligned}
SR_{int} &= \left.\frac{dV_o}{dt}\right|_{max} = \frac{I_{x(max)}}{C_c} = \frac{I_{SS}}{C_c} \\
&= \frac{I_{SS}}{g_{m1}} \times \frac{g_{m1}}{C_c} = \frac{I_{SS}}{g_{m1}} \times \omega_u \\
&= (V_{GS1} - V_{t1}) \times \omega_u \\
&= V_{ov1} \times \omega_u
\end{aligned}
$$

The *external slew rate* is limited by the available current to charge and discharge C_2. Thus,

$$SR_{ext} = \frac{I_{D7} - I_x(max)}{C_2} = \frac{I_{D7} - I_{SS}}{C_2}$$

Settling time

The frequency response and step response of a single-pole amplifier is

$$A(s) = \frac{A_o}{1 + s/\omega_p} \qquad V_o(t) = A_o\left(1 - e^{-\omega_p t}\right)$$

The settling time can be written as

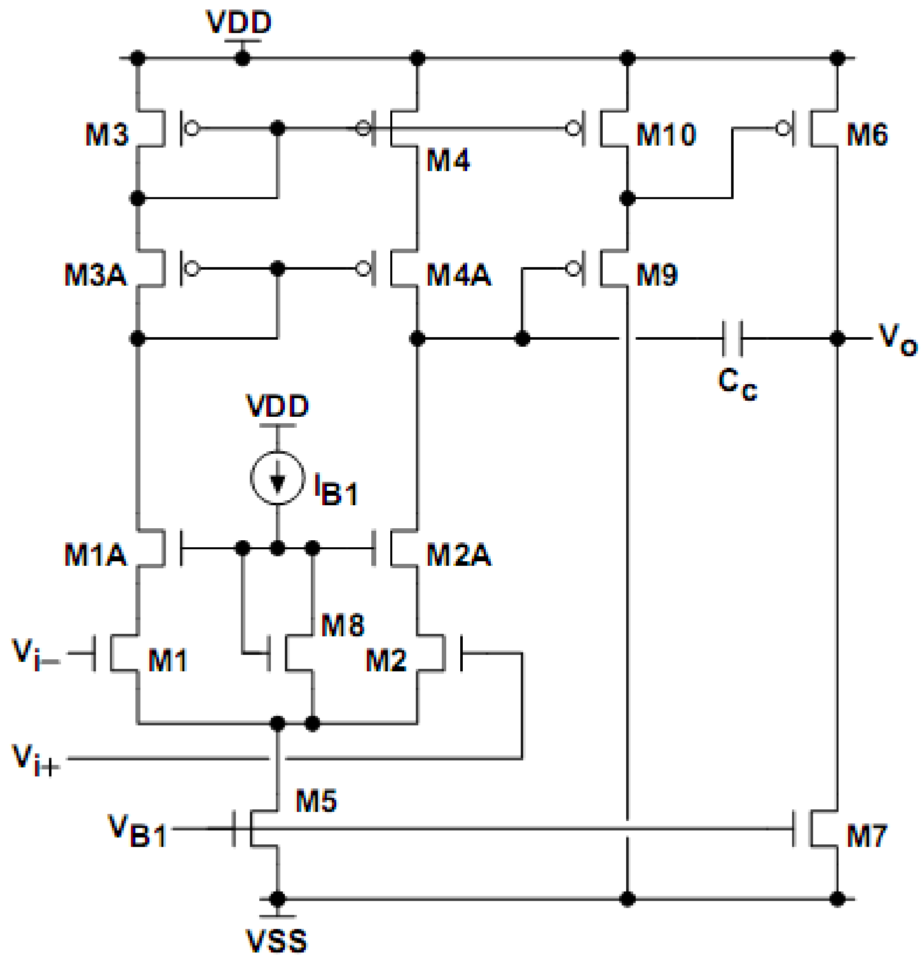
$$t_s(\epsilon) = \frac{1}{\omega_p}\ln\frac{1}{\epsilon} = \frac{A_o}{\omega_u}\ln\frac{1}{\epsilon}$$

- $\omega_u = A_o \cdot \omega_p$ is the dominant-pole unity-gain frequency.
- $\epsilon = 1 - |V_o(t_s)/A_o|$ is the error when settling occurs.

The 10% to 90% rise time is

$$t_r = \frac{1}{\omega_p}\ln(9) = \frac{2.2}{\omega_p} = \frac{0.35}{f_p} \qquad \omega_p = 2\pi f_p$$

Two-Stage cascode Operational Amplifier

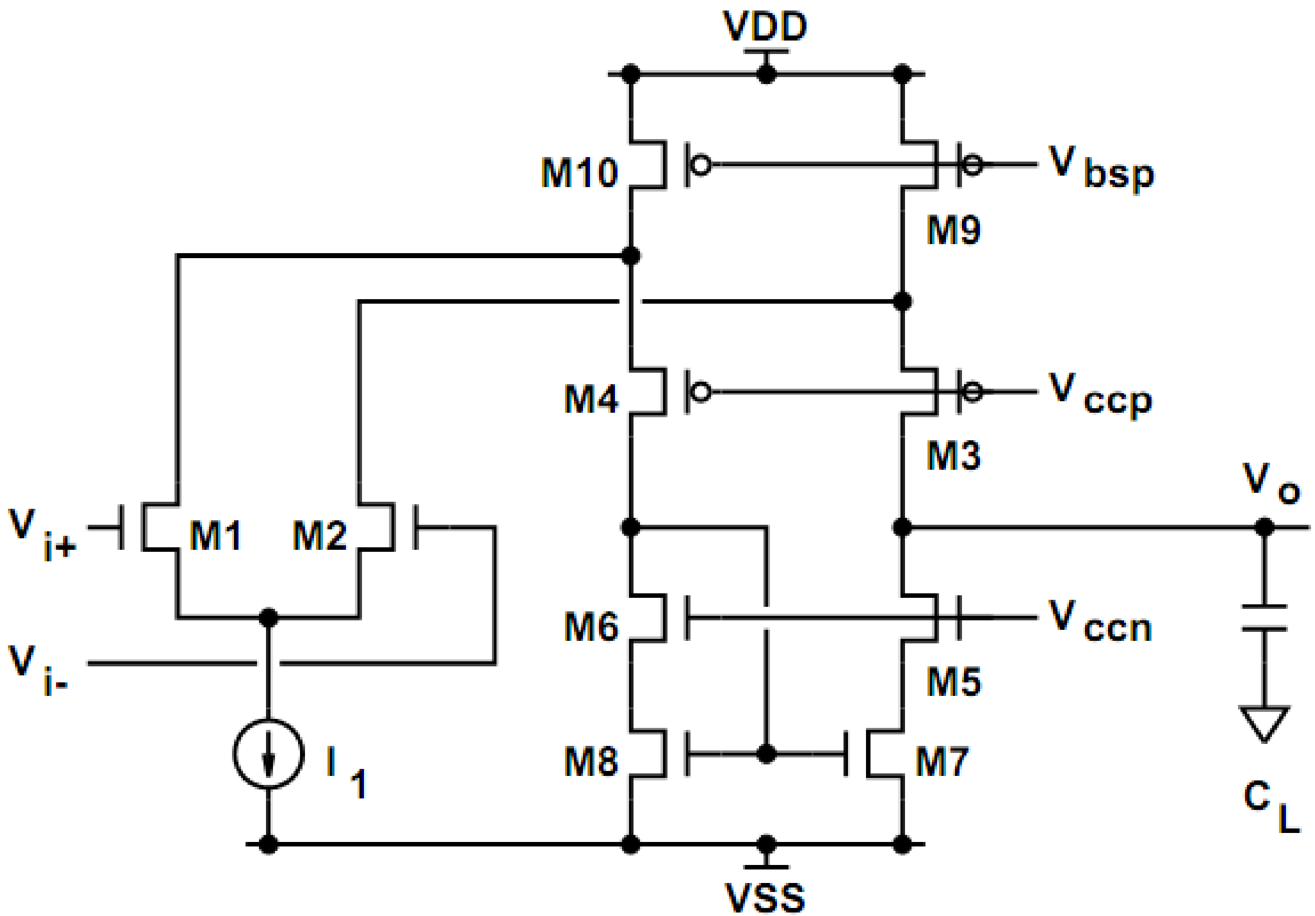


- The volage gain $A_v \propto (g_m r_o)^3$.
- Size M8 so that

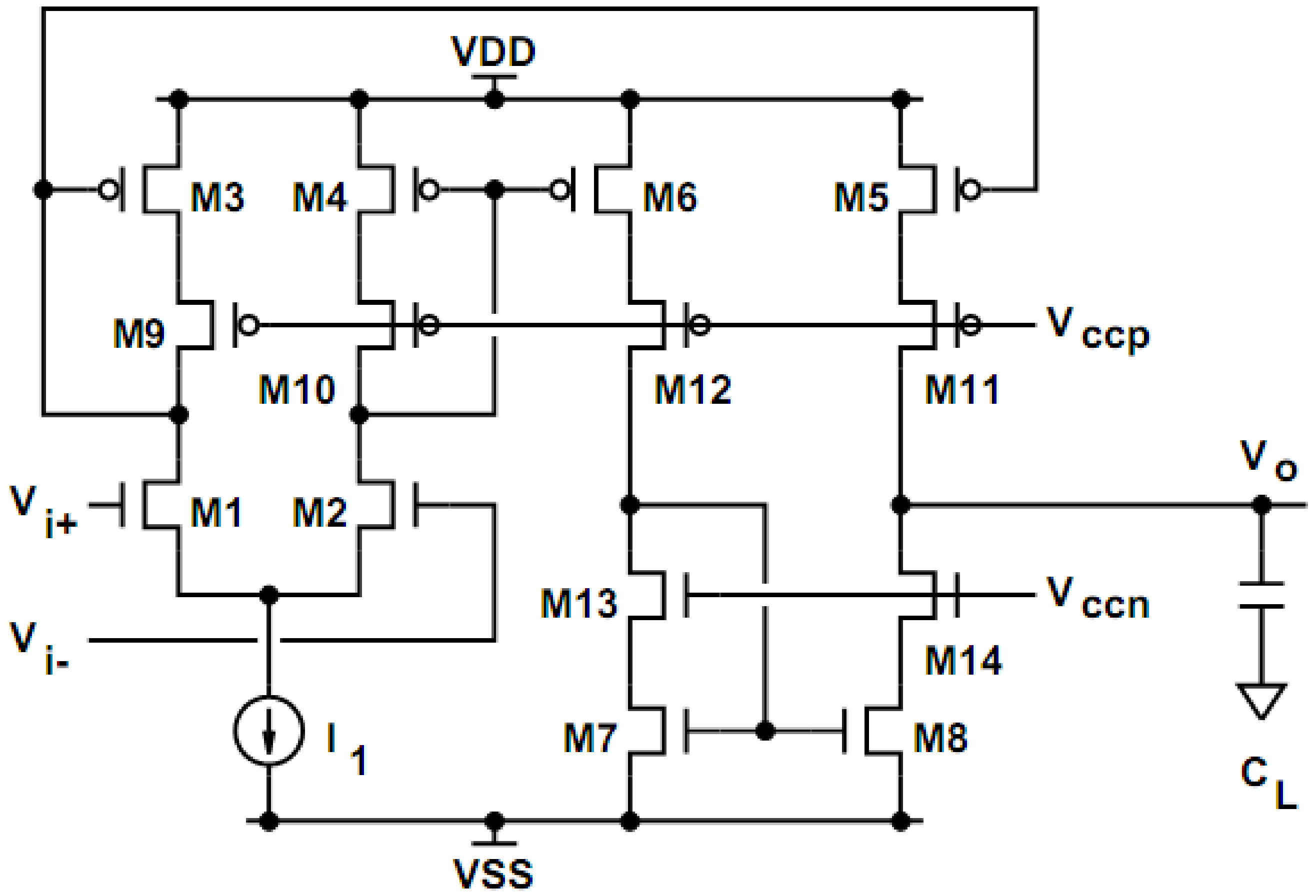
$$V_{DS1} = V_{DS2} \simeq V_{DSAT}$$

- Input common-mode range is reduced by cascodes.
- The additional poles are non-dominant and located near ω_T.
- The 2nd stage can also use cascodes.

Folded-Cascode Operational Amplifier



Current-mirror opamp



Current-mirror opamp

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_6 = \frac{1}{K}\left(\frac{W}{L}\right)_5 \qquad \left(\frac{W}{L}\right)_7 = \frac{1}{K}\left(\frac{W}{L}\right)_8$$

$$I_{D1,D2} = I_{D3,D4} = I_{D6} = I_{D7} = \frac{1}{K}I_{D5} = \frac{1}{K}I_{D8} = \frac{1}{2}I_1 \qquad SR = \frac{KI_1}{C_L}$$

$$A_v(0) = Kg_{m1}R_o \qquad R_o = \frac{1}{\frac{g_{o5}}{g_{m11}r_{o11}} + \frac{g_{o8}}{g_{m14}r_{o14}}} \qquad p_1 = -\frac{1}{R_oC_L} \qquad \omega_u = \frac{Kg_{m1}}{C_L}$$

- For a given power dissipation, the current-mirror opamps have larger bandwidth and SR than the folded-cascode opamps. But they also suffer from larger thermal noise.
- For small C_L, K may have to be reduced to prevent the nondominant poles from degrading the phase margin.
- A practical upper limit on K is around 5. For a general-purpose opamp, $K \simeq 2$.