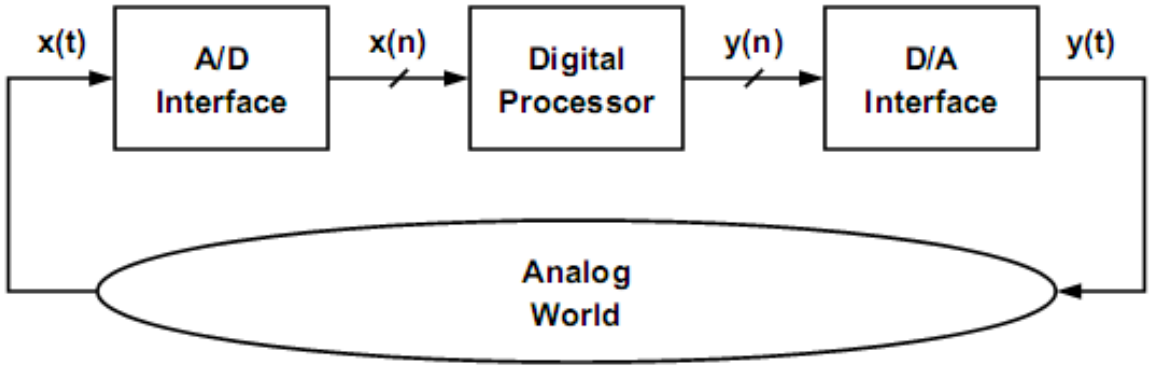
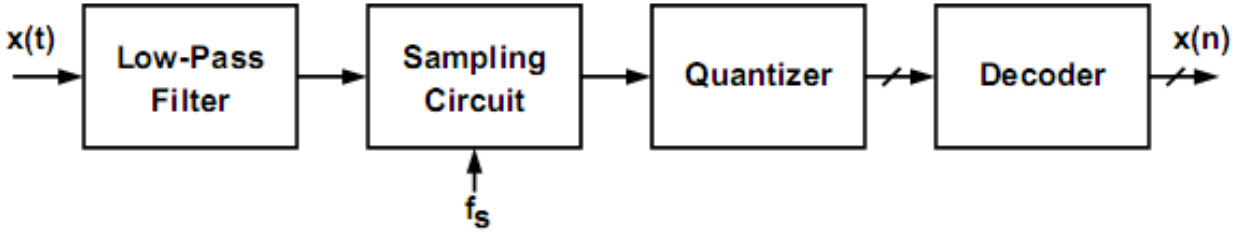
Digital-to-analog converters

Apinunt Thanachayanont

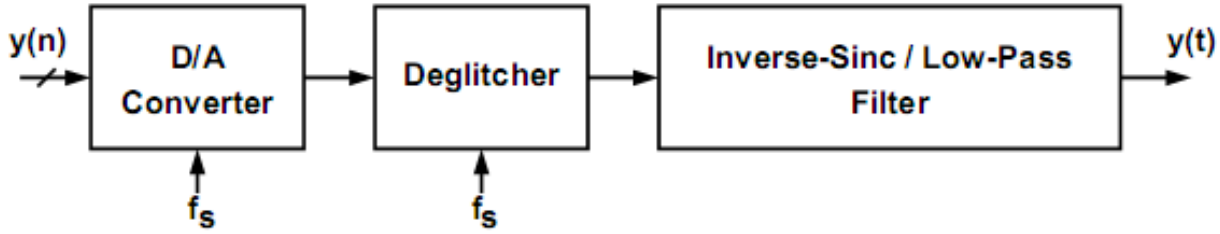
A/D and D/A interfaces



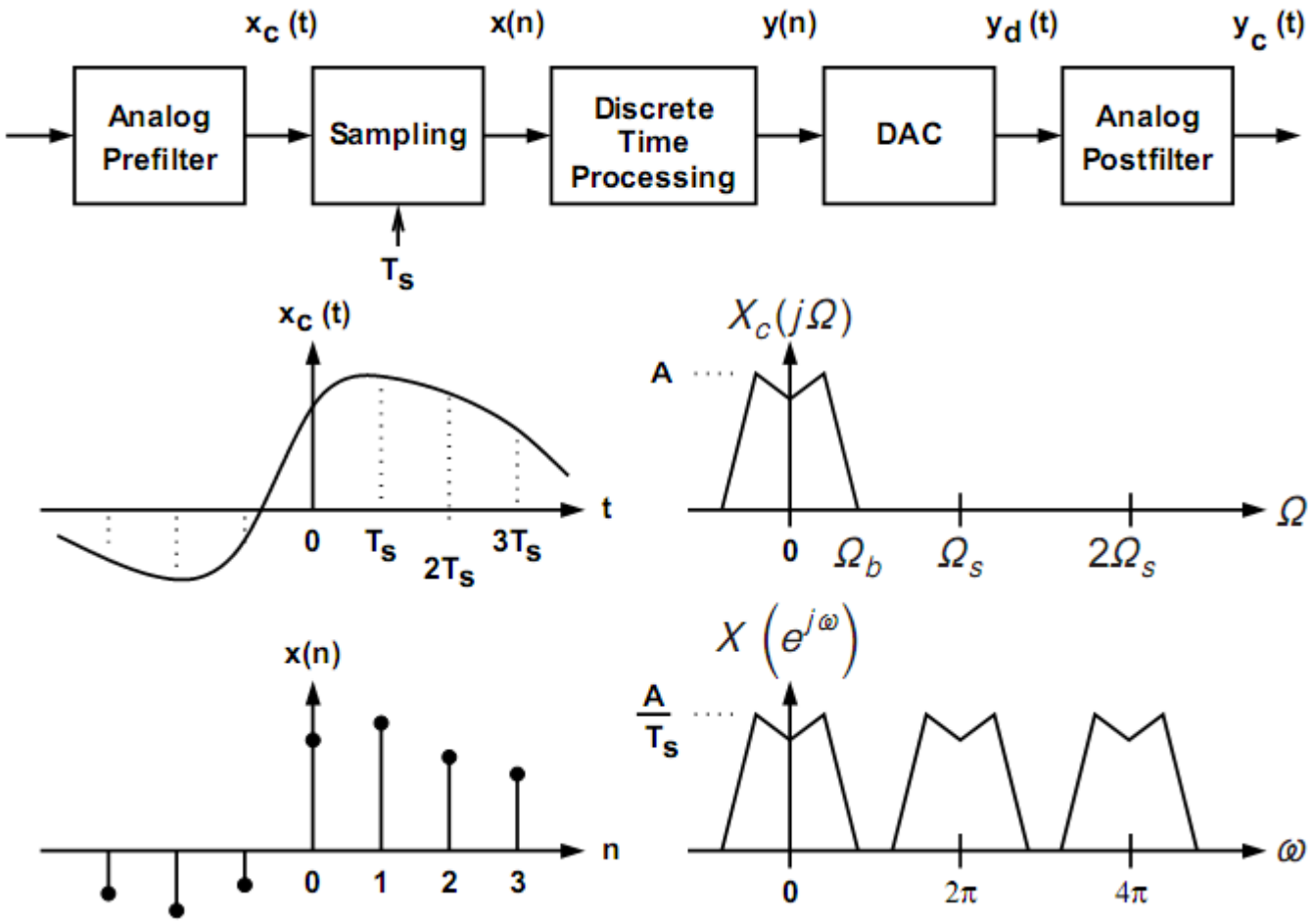
Analog-to-Digital Interface



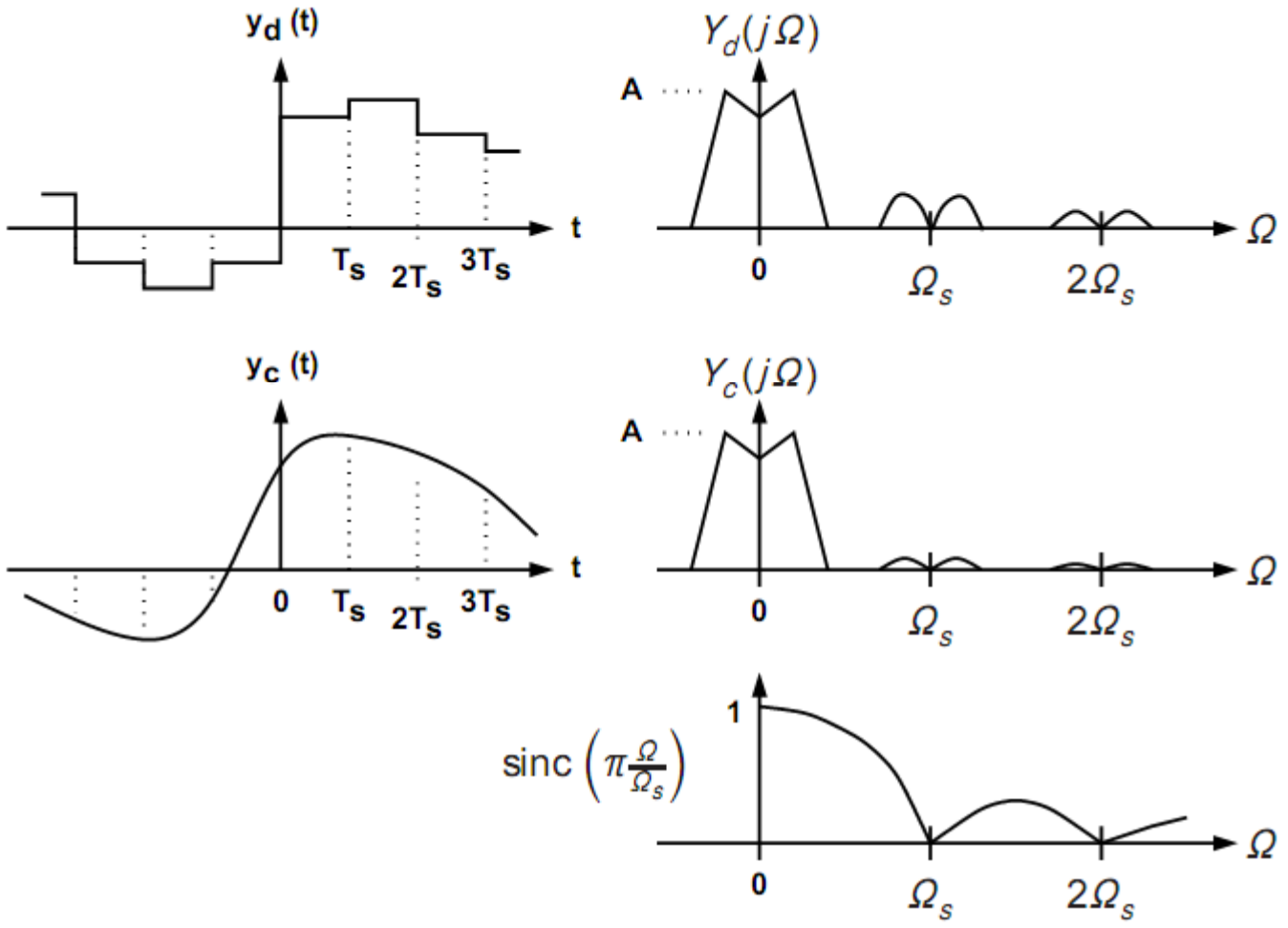
Digital-to-Analog Interface



Continuous-to-discrete conversion



Discrete-to-continuous conversion



Block diagram of D/A converter

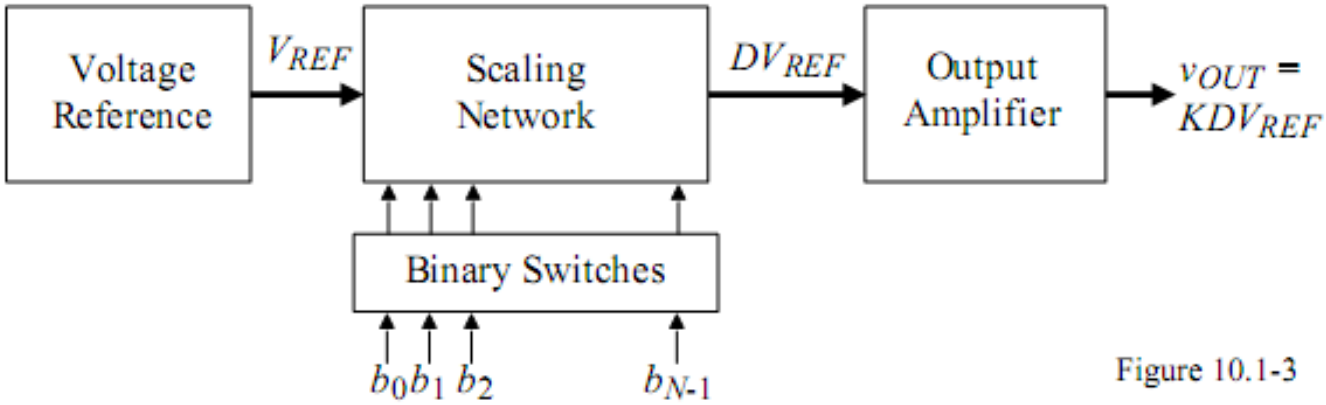


Figure 10.1-3

b_0 is the most significant bit (MSB)

The MSB is the bit that has the most (largest) influence on the analog output

b_{N-1} is the least significant bit (LSB)

The LSB is the bit that has the least (smallest) influence on the analog output

Input-output characteristic of DAC

- 3-bit DAC

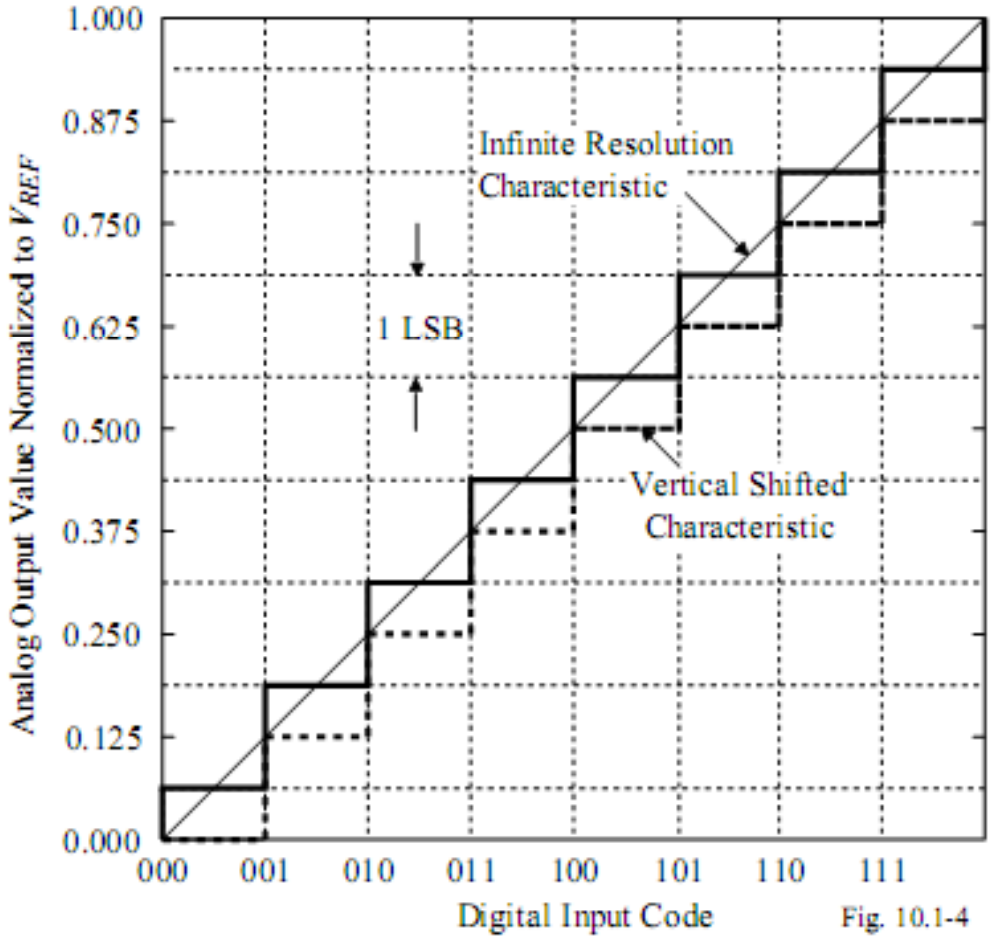
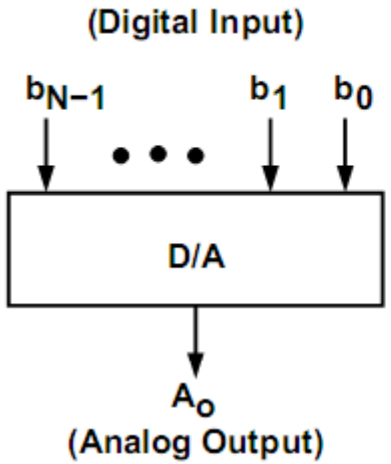
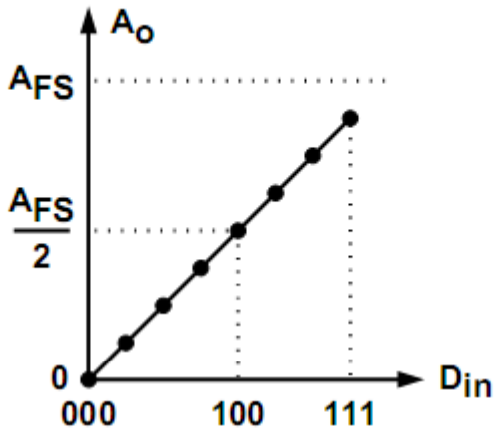


Fig. 10.1-4

D/A transfer characteristic





A_{FS} = Full-Scale Output

$$\Delta = \text{LSB} = \text{Step Size} = \frac{A_{FS}}{2^N}$$

$$\begin{aligned} A_o &= \Delta \times D_{in} \\ &= \Delta \times \left[b_{N-1}2^{N-1} + \cdots + b_1 2^1 + b_0 2^0\right] \\ &= A_{FS} \times \left[b_{N-1}2^{-1} + \cdots + b_1 2^{-(N-1)} + b_0 2^{-N}\right] \end{aligned}$$

- In some applications, relationship between D_{in} and A_o can be nonlinear.
- D_{in} may use other coding scheme such as offset binary or 2's complement.

D/A performance metrics: Static

- Resolution: number of bits (N), analog 1 LSB step (Δ).
- Offset error.
- Gain error.
- Integral nonlinearity (INL).
- Differential nonlinearity (DNL).
- Monotonicity.
  - Monotonicity can be assumed if the DNL > −1 LSB for all input codes.
- Stability.
  - Variation with time, temperature, and supply voltage.

Static characteristics of DAC

- Resolution of the DAC is equal to the number of bits in the applied digital input word.
- The Full Scale (FS):
  - FS = Analog output when all bits are 1 - Analog output all bits are 0

$$FS = (V_{REF} - \frac{V_{REF}}{2^N}) - 0 = V_{REF}\left(1 - \frac{1}{2^N}\right)$$

  - Full scale range = $FSR = \lim_{N \to \infty} FS = V_{REF}$
- Quantization Noise is the inherent uncertainty in digitizing an analog value with a finite resolution converter.

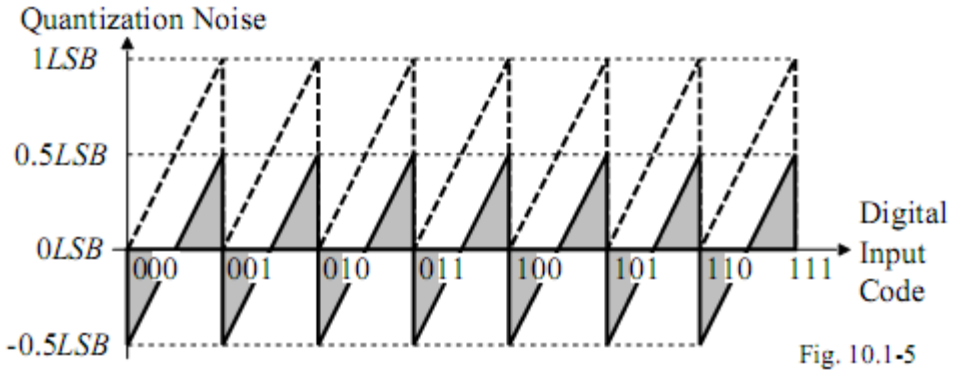
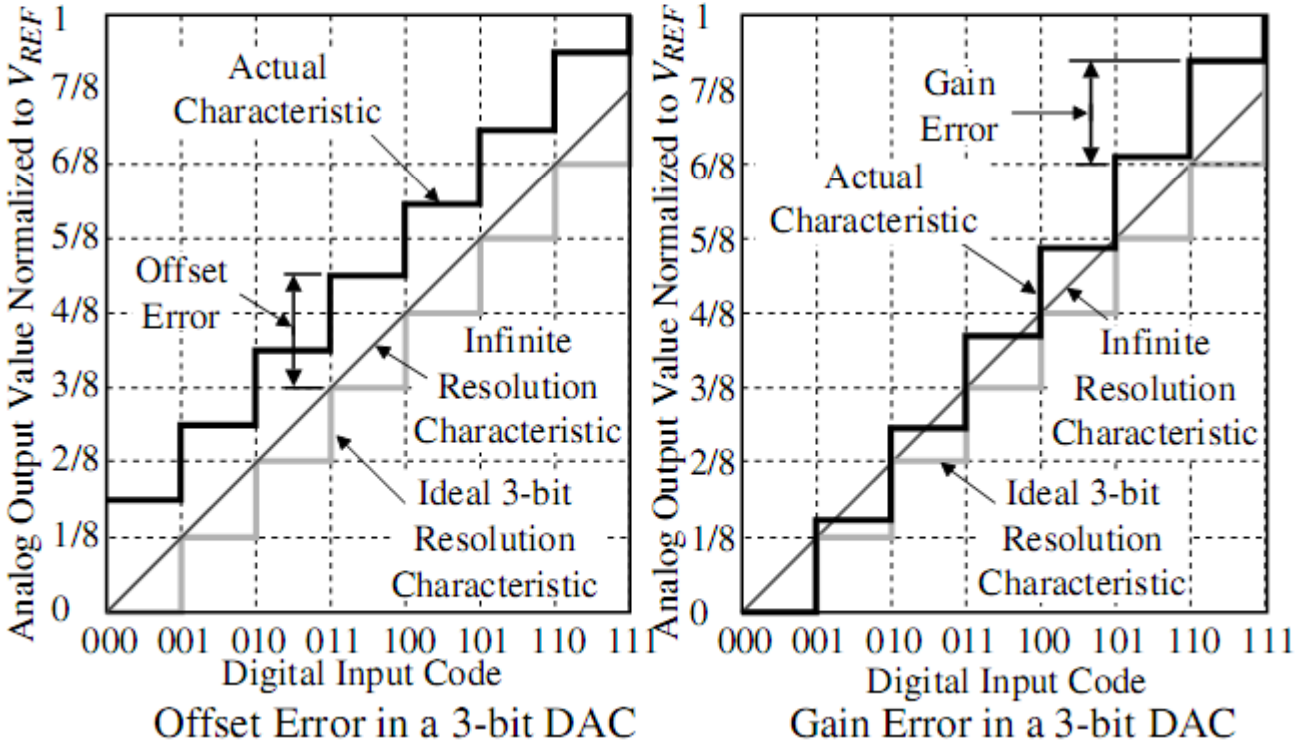


Fig. 10.1-5

Non-idealities of DAC

An *offset error* is a constant difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured at any vertical jump.

A *gain error* is the difference between the slope of the actual finite resolution and the ideal finite resolution characteristic measured at the right-most vertical jump.



Offset Error in a 3-bit DAC

Gain Error in a 3-bit DAC

INL & DNL

- *Integral Nonlinearity* (*INL*) is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically (% or *LSB*).
- *Differential Nonlinearity* (*DNL*) is a measure of the separation between adjacent levels measured at each vertical jump (% or *LSB*).

$$DNL = V_{cx} - V_s = \left(\frac{V_{cx} - V_s}{V_s}\right) V_s = \left(\frac{V_{cx}}{V_s} - 1\right) LSBs$$

where V_{cx} is the actual voltage change on a bit-to-bit basis and V_s is the ideal *LSB* change of $(V_{FSR}/2^N)$

Example of a 3-bit DAC:

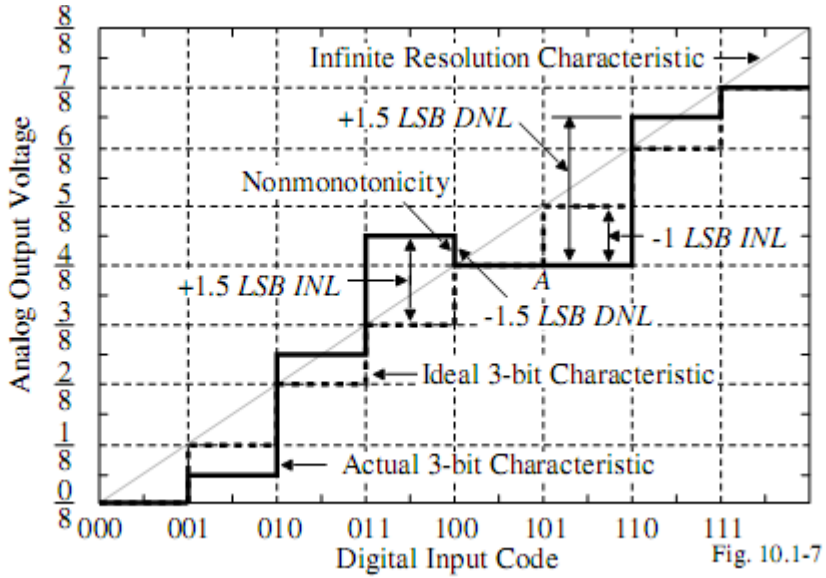


Fig. 10.1-7

INL & DNL of 4-bit DAC

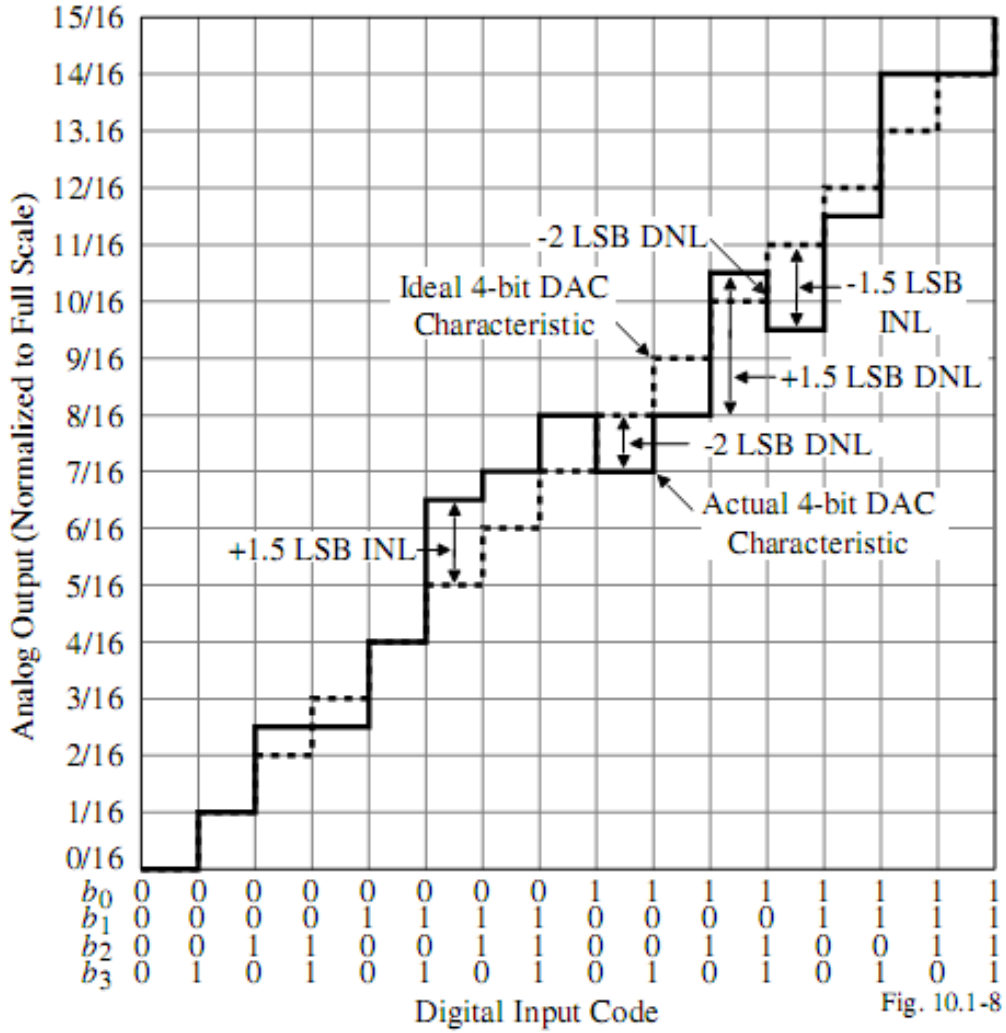


Fig. 10.1-8

D/A performance metrics: Dynamic

- Sampling rate.
- Settling time.
  - Settling time is the time taken by the D/A output to settle within some specified error band (typically $\pm\frac{1}{2}$ LSB).
  - The settling time is primarily dominated by the settling of the MSB contribution.
- Glitch impulse area (glitch energy).
  - Glitches is the output transient spikes during the conversion process.
  - Glitches are caused by the unequal delays in switching various signal sources within the converter.
- Dynamic range: SNR_{max}, SNDR, SFDR.

Dynamic characteristics of DAC

- *Dynamic Range* (*DR*) of a DAC is the ratio of the *FS*R to the smallest difference that can be resolved (i.e. an *LSB*)

$$DR = \frac{FSR}{LSB \text{ change}} = \frac{FSR}{(FSR/2^N)} = 2^N$$

or in terms of decibels

$$DR(\text{dB}) = 6.02N \text{ (dB)}$$

- *Signal-to-noise ratio* (*SNR*) for the DAC is the ratio of the full scale value to the *rms* value of the quantization noise.

$$rms(\text{quantization noise}) = \sqrt{\frac{1}{T}\int_0^T LSB^2\left(\frac{t}{T} - 0.5\right)^2 dt} = \frac{LSB}{\sqrt{12}} = \frac{FSR}{2^N\sqrt{12}}$$

$$\therefore \quad SNR = \frac{v_{OUT}(rms)}{(FSR/\sqrt{12}\,2^N)}$$

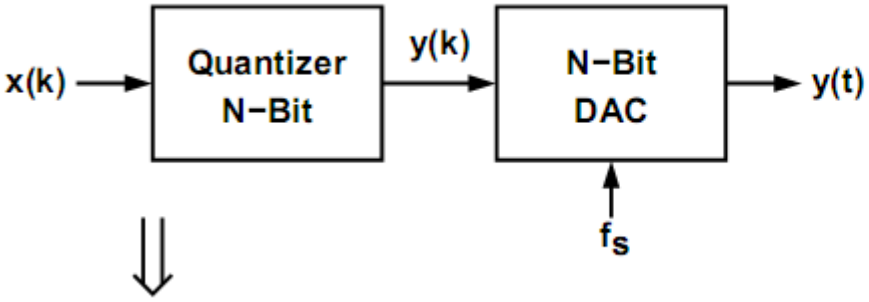
- *Maximum SNR* (SNR_{max}) for a sinusoid is defined as

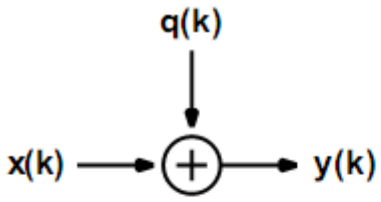
$$SNR_{max} = \frac{v_{OUT_{max}}(rms)}{(FSR/\sqrt{12}\,2^N)} = \frac{FSR/(2\sqrt{2})}{FSR/(\sqrt{12}\,2^N)} = \frac{\sqrt{6}\,2^N}{2}$$

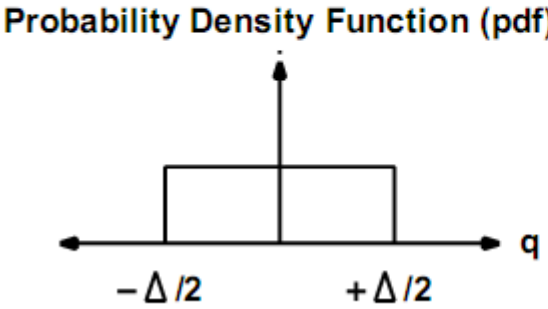
or in terms of decibels

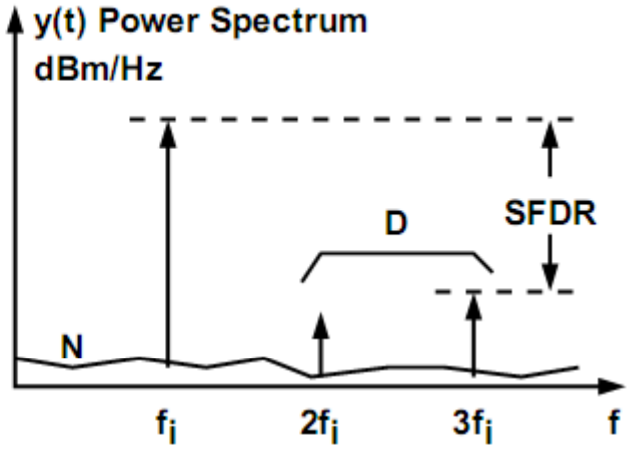
$$SNR_{max}(\text{dB}) = 20log_{10}\left(\frac{\sqrt{6}2^N}{2}\right) = 10\,log_{10}(6)+20\,log_{10}(2^N)-20\,log_{10}(2) = 1.76 + 6.02N \text{ dB}$$

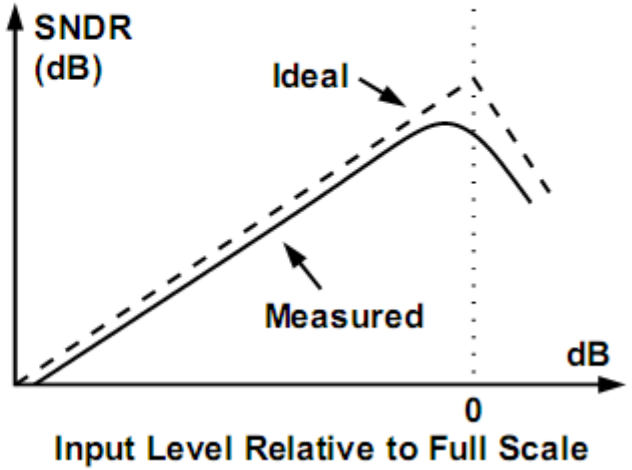
Dynamic range











Dynamic range

- The ratio between f_s and f_i should be irrational.
- In the discrete-time domain, noise power of $q(k)$ is assumed to be uniformly distributed between $-\Omega_s/2$ and $+\Omega_s/2$. The power density is $\Delta^2/(12\Omega_s)$.
- The *spurious free dynamic range* (SFDR) is the ratio of the fundamental signal component to the largest distortion component when $A = A_{FS}/2$.
- *Signal-to-noise ration* (SNR) and *signal-to-noise plus distortion ratio* (SNDR) are defined as

$$\text{SNR} = \frac{S}{N} \qquad \text{SNDR} = \frac{S}{N+D}$$

  In finding the total noise power, the noise bandwidth need to be specified.
- Effective number of bits (ENOB) and dynamic range (DR) are defined as

$$\text{ENOB} = \frac{\text{SNDR} - 1.76}{6.02} \qquad \text{DR} = \frac{S_{max}}{S_{min}@\text{SNR=0dB}}$$

DAC

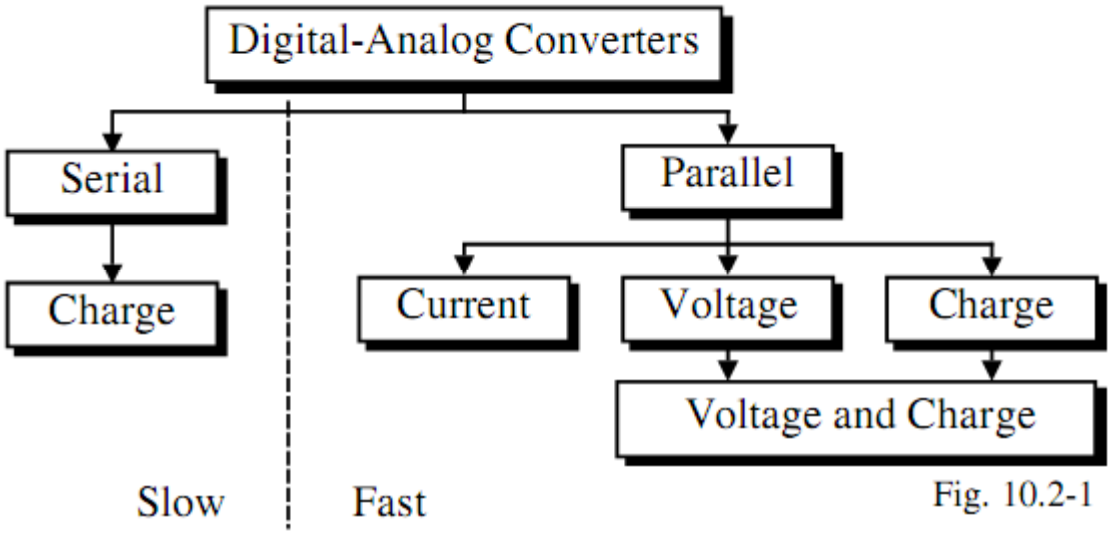

Digital-Analog Converters
Serial
Charge
Parallel
Current
Voltage
Charge
Voltage and Charge
Slow
Fast

Fig. 10.2-1

Voltage-scaling DAC

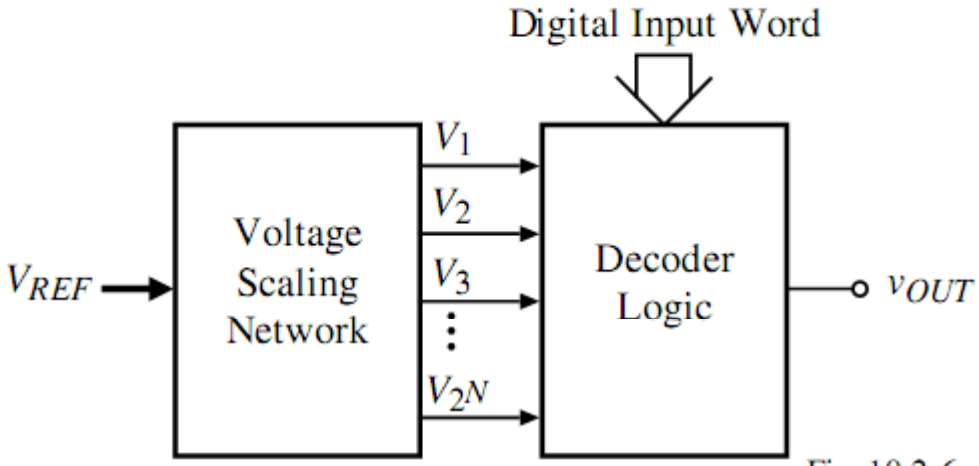
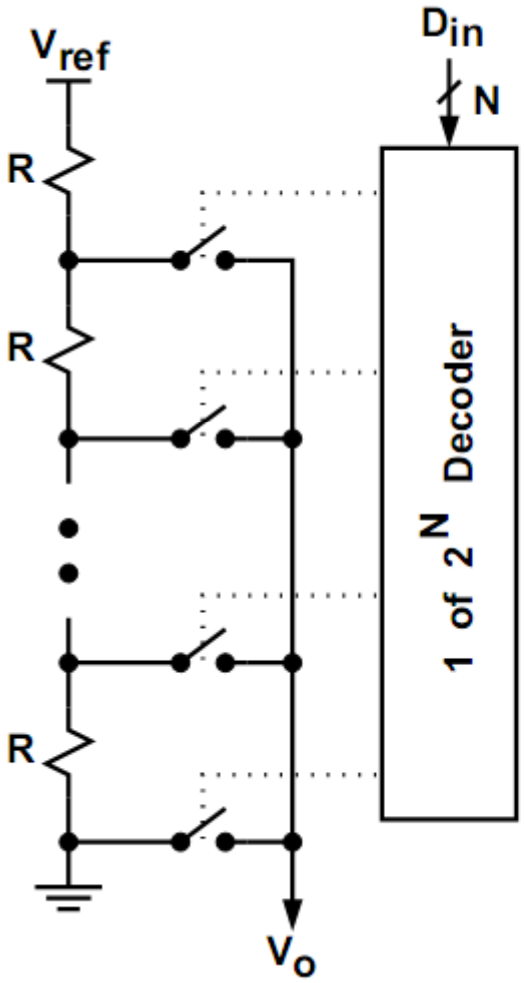


Fig. 10.2-6

Operation:

Creates all possible values of the analog output then uses a decoding network to determine which voltage to select based on the digital input word.

Resistor-string DAC with digital decoding



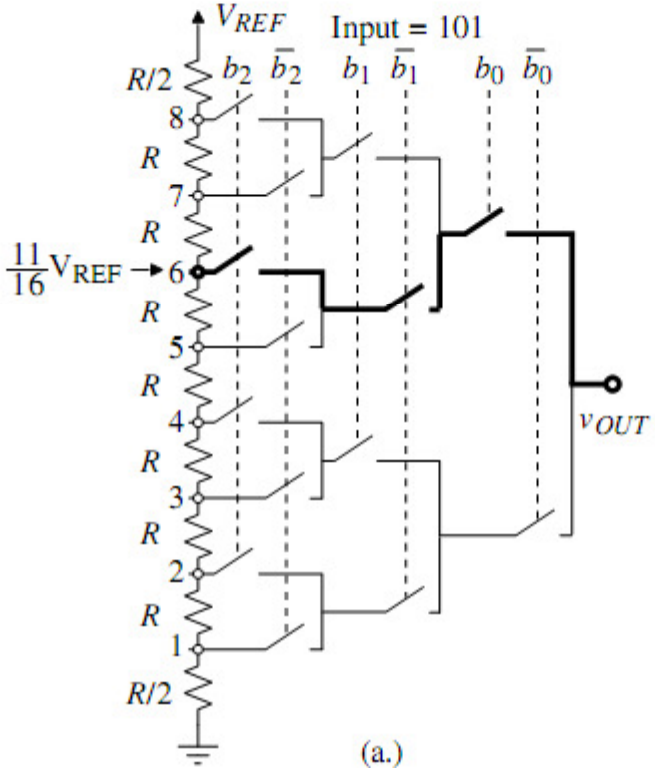
- Inherently monotonic.
- DNL depend on local matching of neighboring R's.
- INL depends on global matching of the R-string.
- No resistive load at V_o.
- The worst-case time constant occurs a the midpoint of the R-string.
- Large capacitive loading at V_o.

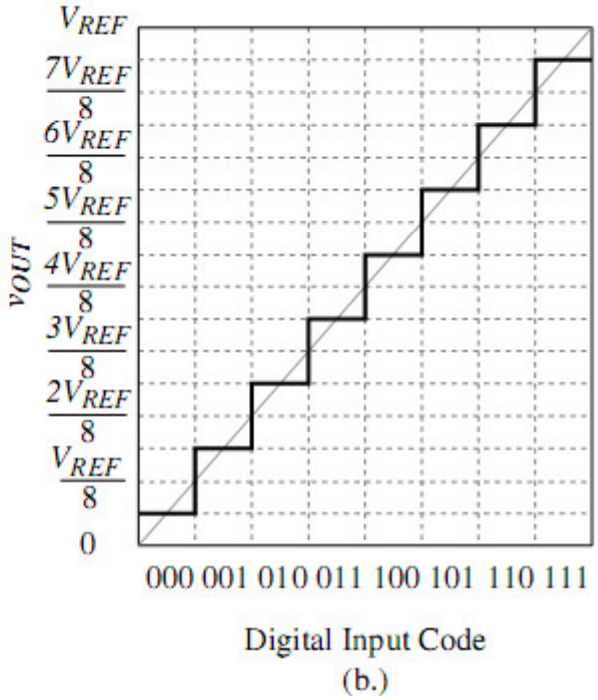
Resistor-string DAC with binary-tree decoding

The voltage at any tap can be expressed as: $v_{OUT} = \frac{V_{REF}}{8}(n - 0.5) = \frac{V_{REF}}{16}(2n - 1)$

Attributes:

- Guaranteed monotonic
- Compatible with CMOS technology
- Large area if N is large
- Sensitive to parasitics
- Requires a buffer
- Large current can flow through the resistor string.





Current-scaling DAC

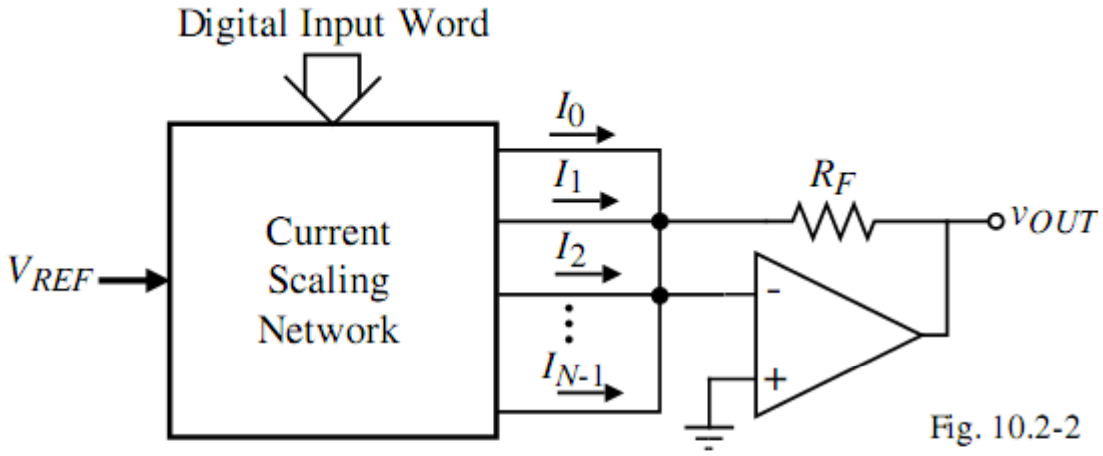


Fig. 10.2-2

The output voltage can be expressed as

$$V_{OUT} = -R_F(I_0 + I_1 + I_2 + \cdots + I_{N-1})$$

where the currents I_0, I_1, I_2, ... are binary weighted currents.

Binary-weighted resistor DAC

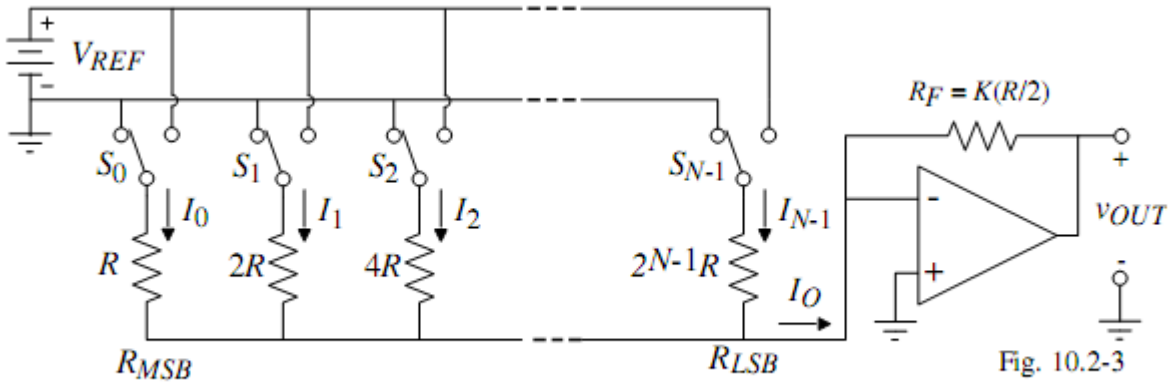


Fig. 10.2-3

Comments:

1.) R_F can be used to scale the gain of the DAC. If $R_F = KR/2$, then

$$v_{OUT} = -R_F I_O = \frac{-KR}{2}\left(\frac{b_0}{R} + \frac{b_1}{2R} + \frac{b_2}{4R} + \cdots + \frac{b_{N-1}}{2^{N-1}R}\right)V_{REF} \Rightarrow v_{OUT} = -K\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \cdots + \frac{b_{N-1}}{2^N}\right)V_{REF}$$

where b_i is 1 if switch S_i is connected toV_{REF} or 0 if switch S_i is connected to ground.

2.) Component spread value $= \dfrac{R_{MSB}}{R_{LSB}} = \dfrac{R}{2^{N-1}R} = \dfrac{1}{2^{N-1}}$

3.) Attributes:

Insensitive to parasitics ⇒ fast	Large component spread value
Trimming required for large values of N	Nonmonotonic

R-2R ladder DAC

Use of the R-2R concept to avoid large element spreads:

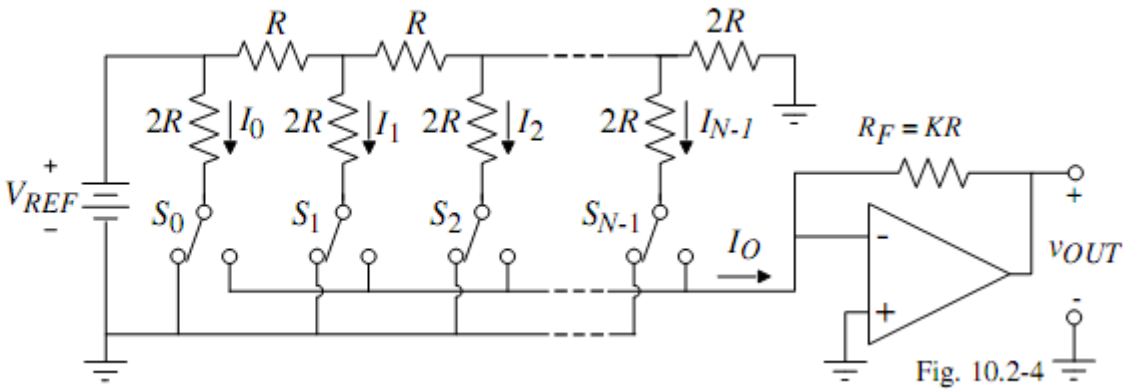


Fig. 10.2-4

How does the R-2R ladder work?

"The resistance seen to the right of any of the vertical $2R$ resistors is $2R$."

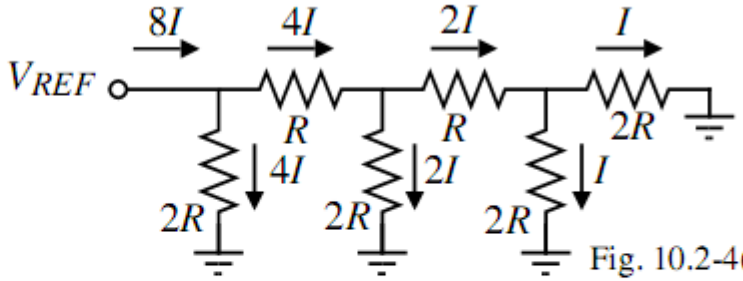


Fig. 10.2-4(2R-R)

Attributes:

- Not sensitive to parasitics (currents through the resistors never change as S_i is varied)
- Small element spread. Resistors made from same unit ($2R$ consist of two in series or R consists of two in parallel)
- Not monotonic

Current-steering DAC

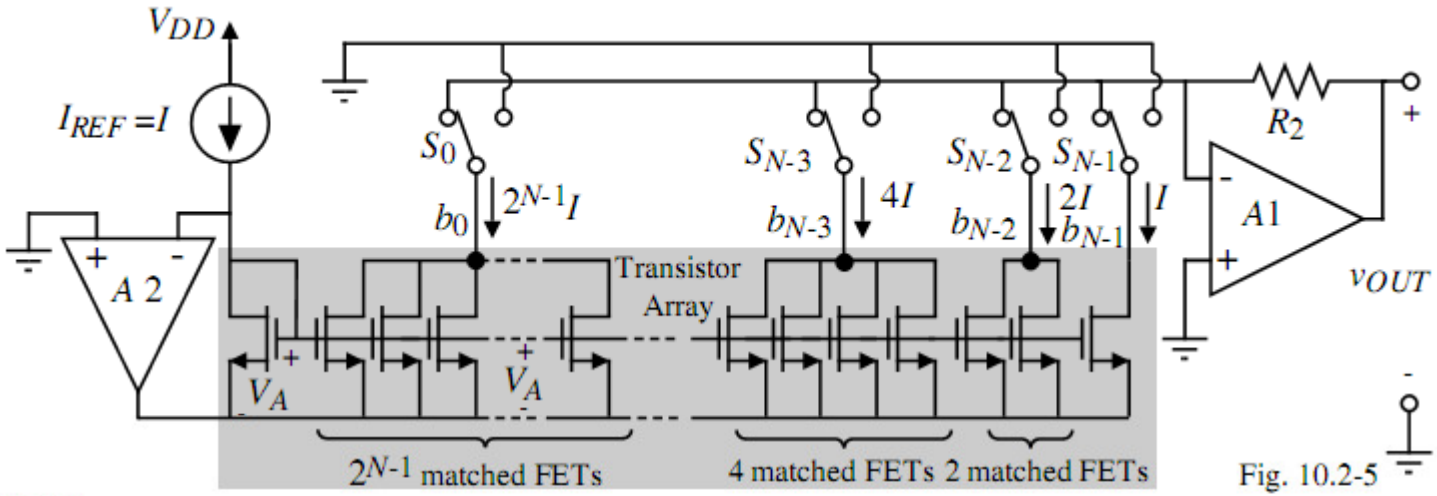


Fig. 10.2-5

Operation:

$$v_{OUT} = R_2(b_{N-1}\cdot I + b_{N-2}\cdot 2I + b_{N-3}\cdot 4I + \cdots + b_0\cdot 2^{N-1}\cdot I)$$

If $I = I_{REF} = \dfrac{V_{REF}}{2^N R_2}$,

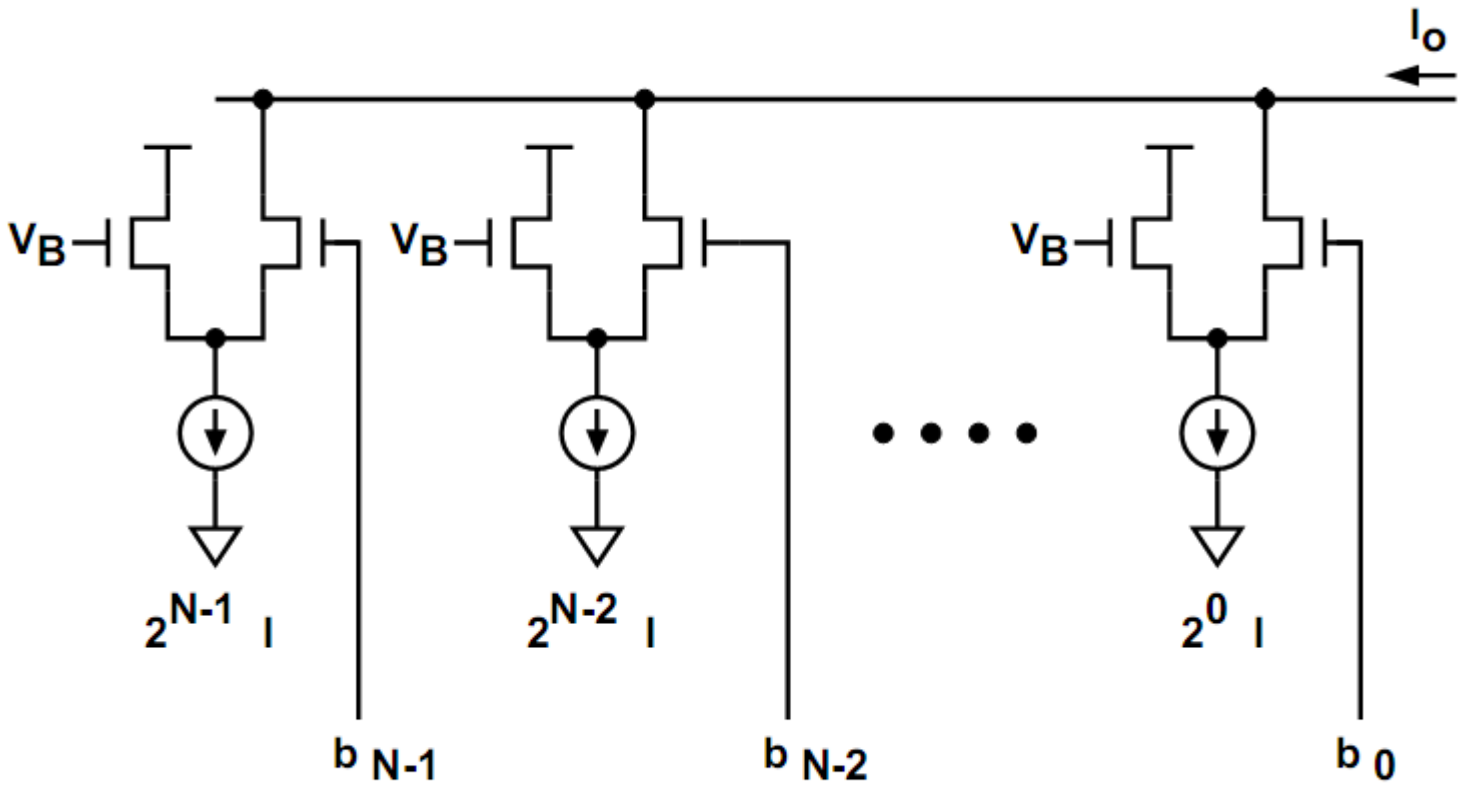
then

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \cdots + \frac{b_{N-3}}{2^{N-2}} + \frac{b_{N-2}}{2^{N-1}} + \frac{b_{N-1}}{2^N}\right) V_{REF}$$

Attributes:

Fast (no floating nodes) and not monotonic Accuracy of MSB greater than LSBs

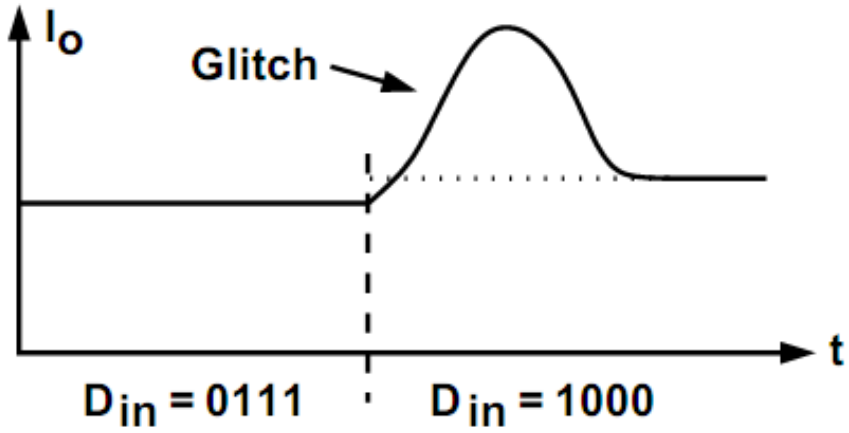
Binary-weighted current-steering DAC



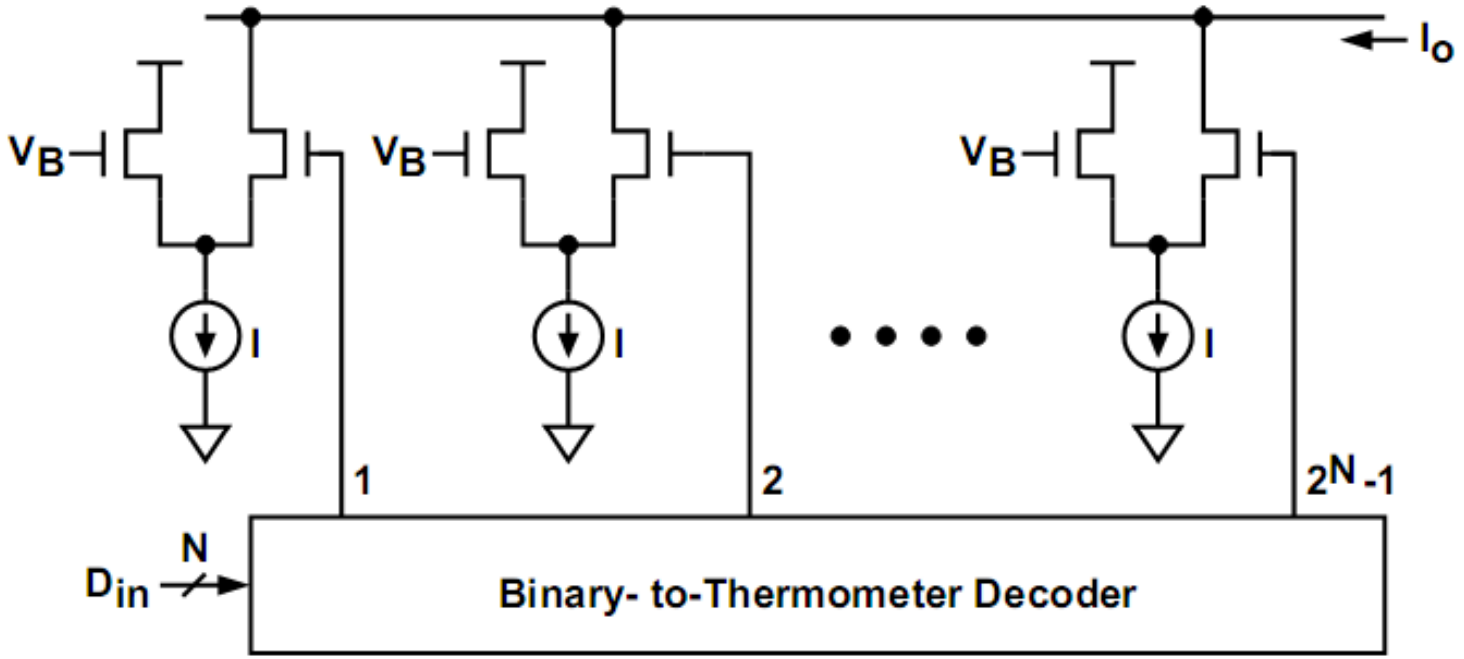
$$I_o = I \cdot \left(b_{N-1} \cdot 2^{N-1} + b_{N-2} \cdot 2^{N-2} + \cdots + b_1 \cdot 2^1 + b_0 \cdot 2^0 \right)$$

Binary-weighted current-steering DAC

- Fast.
- Monotonicity is not guaranteed.
- Potentially large glitches due to timing skews.
- Latches are often used to synchronize b_{N-1}, b_{N-2}, ...
- R_o of the current sources can cause nonlinearity.

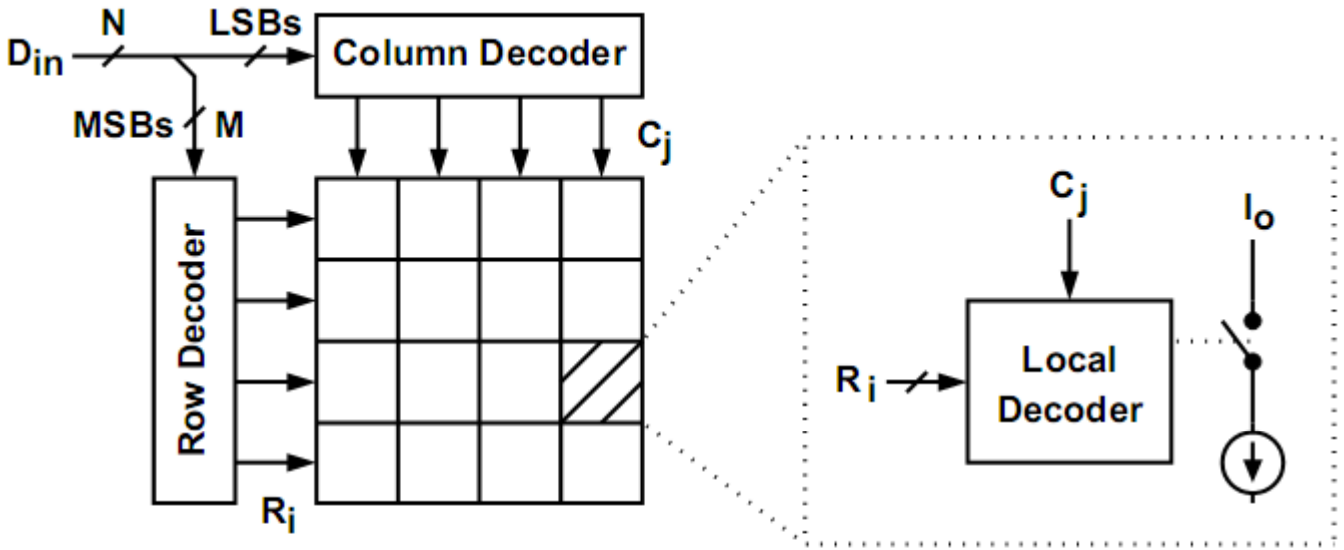


Equally-Weighted Current-Steering DACs



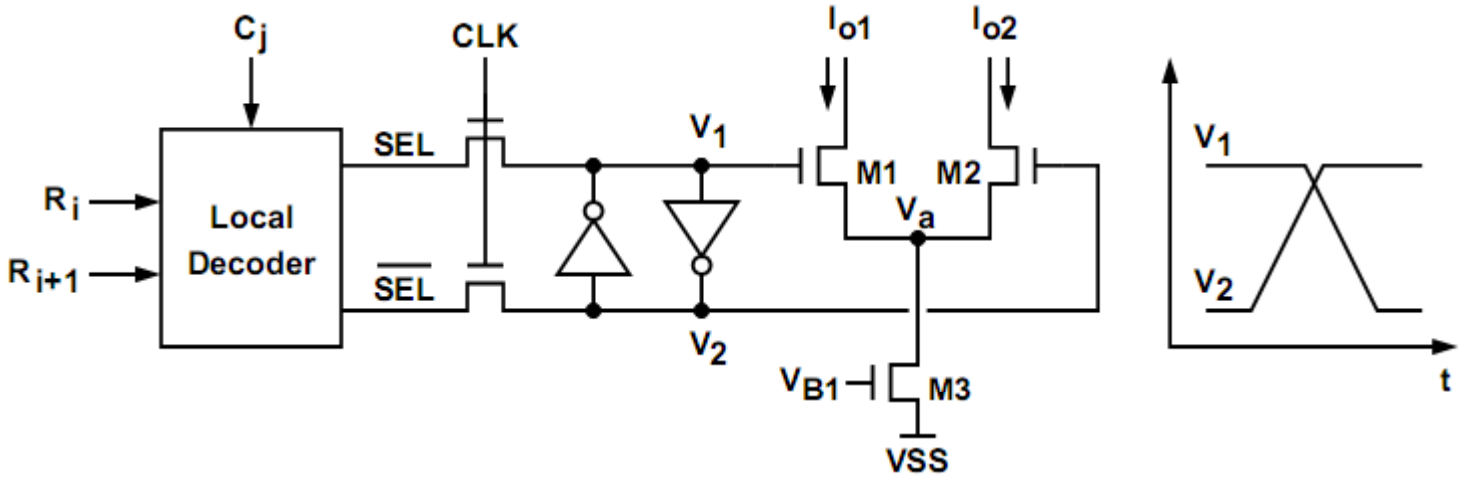
- Inherently monotonic.
- Glitches are reduced. Synchronizing latches may be still required.

Floorplan of a Current-Steering DACs



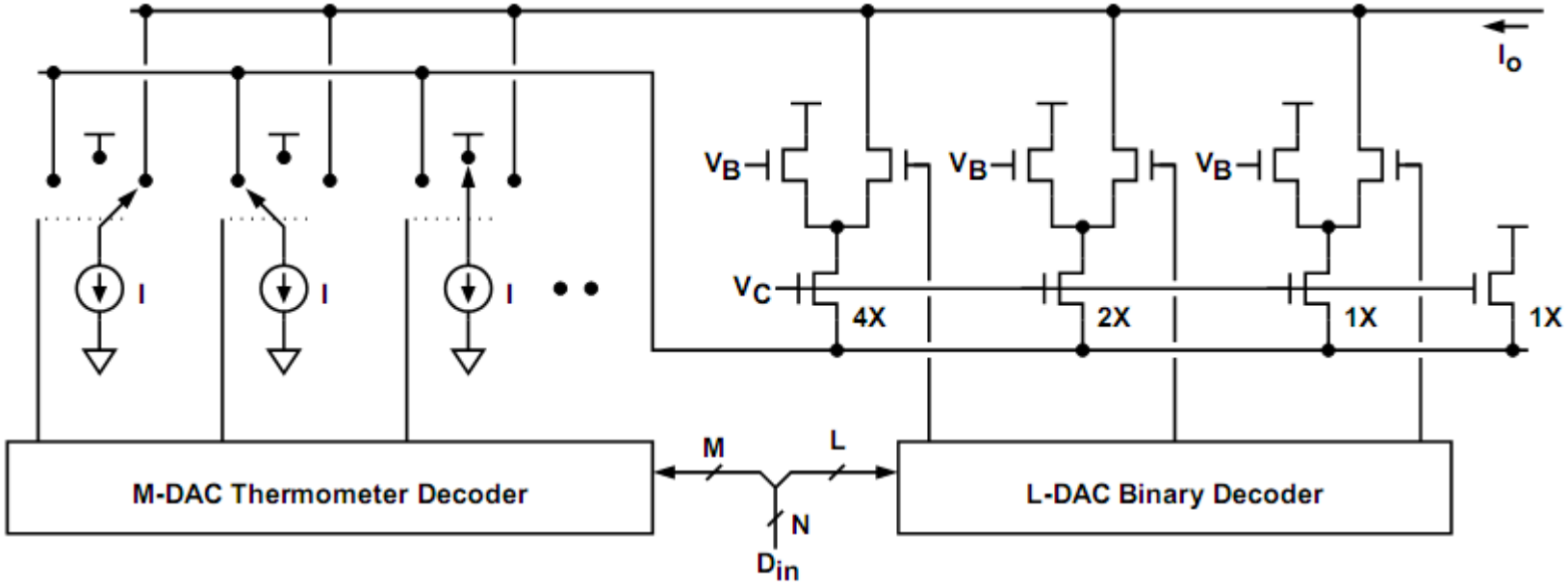
- R_j is a $2^M - 1$ thermometer code, and C_j is a $2^{N-M} - 1$ thermometer code.
- One example of the local decoding is $S = R_{i+1} + R_i \cdot C_j$.
- INL may exhibit the gradient of the unit cell's variations.
- INL can be *dithered* by jumping selection of unit cells.

Current cell example



- The current switch MOSTs, M1 and M2, are in the triode region when fully turned on.
- To minimize voltage fluctuation at V_a, the inverters are sized so that the cross-over voltage of the V_1 and V_2 transient waveforms can turn on both M1 and M2.

Segmented current-steering DAC



- Greatly reduces area for large *N* while ensuring monotonicity (at least for MSBs).
- The L-DAC can be a binary-weighted DAC if its glitches can be tolerated.

Charge-scaling DAC

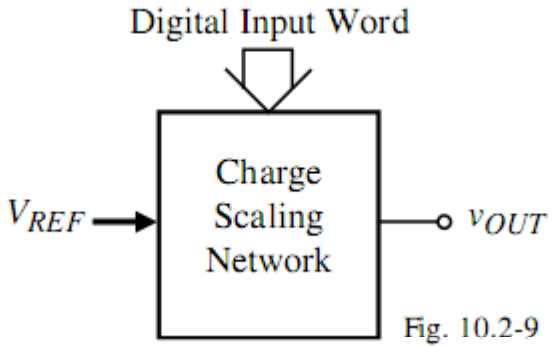


Fig. 10.2-9

General principle is to capacitively attenuate the reference voltage. Capacitive attenuation is simply:

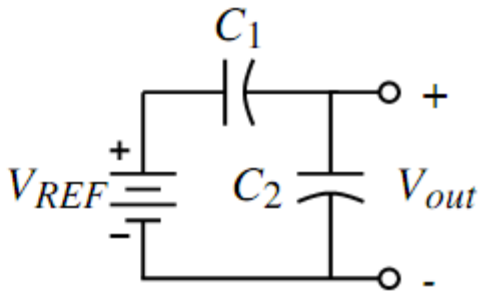


Fig. 10.2-9b

Calculate as if the capacitors were resistors. For example,

$$V_{out} = \frac{\frac{1}{C_2}}{\frac{1}{C_1} + \frac{1}{C_2}} V_{REF} = \frac{C_1}{C_1 + C_2} V_{REF}$$

Charge-scaling DAC

Circuit:

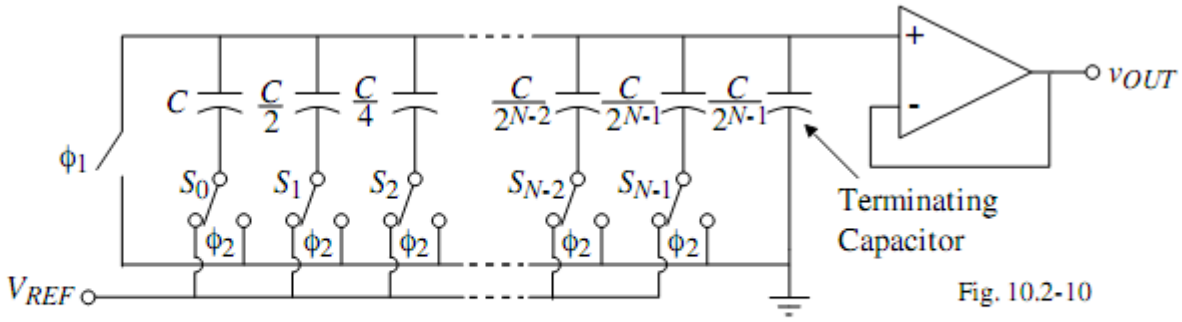


Fig. 10.2-10

Operation:

1.) All switches connected to ground during ϕ_1.

2.) Switch S_i closes to V_{REF} if $b_i = 1$ or to ground if $b_i = 0$.

Equating the charge in the capacitors gives,

$$V_{REF}C_{eq} = V_{REF}\left(b_0C + \frac{b_1C}{2} + \frac{b_2C}{2^2} + \ldots + \frac{b_{N-1}C}{2^{N-1}}\right) = C_{tot}\,v_{OUT} = 2C\,v_{OUT}$$

which gives

$$v_{OUT} = [b_0 2^{-1} + b_1 2^{-2} + b_2 2^{-3} + \ldots + b_{N-1}2^{-N}]V_{REF}$$

Equivalent circuit of the binary-weighted, charge scaling DAC is:

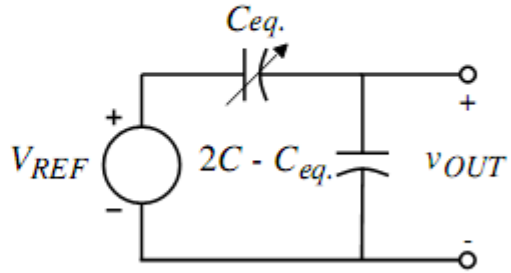


Fig. 10.2-11

Attributes:

- Accurate
- Sensitive to parasitics
- Not monotonic
- Charge feedthrough occurs at turn on of switches

Serial DAC

Serial DACs

- Typically require one clock pulse to convert one bit
- Types considered here are:
  - Charge-redistribution
  - Algorithmic

Charge Redistribution DAC

Implementation:

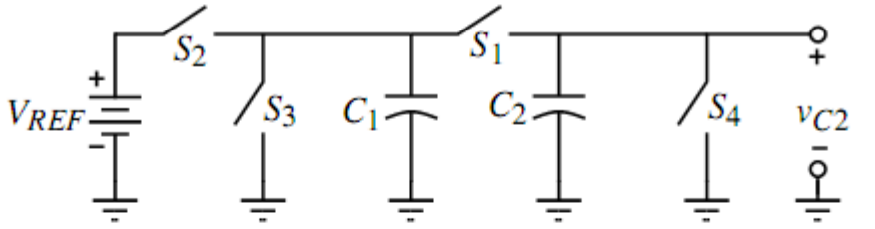


Fig. 10.4-1

Operation:

Switch S_1 is the redistribution switch that parallels C_1 and C_2 sharing their charge

Switch S_2 precharges C_1 to V_{REF} if the ith bit, b_i, is a 1

Switch S_3 discharges C_1 to zero if the ith bit, b_i, is a 0

Switch S_4 is used at the beginning of the conversion process to initially discharge C_2

Conversion always begins with the *LSB* bit and goes to the *MSB* bit.

Operation of charge-redistribution DAC

Assume that $C_1 = C_2$ and that the digital word to be converted is given as $b_0 = 1$, $b_1 = 1$, $b_2 = 0$, and $b_3 = 1$. Follow through the sequence of events that result in the conversion of this digital input word.

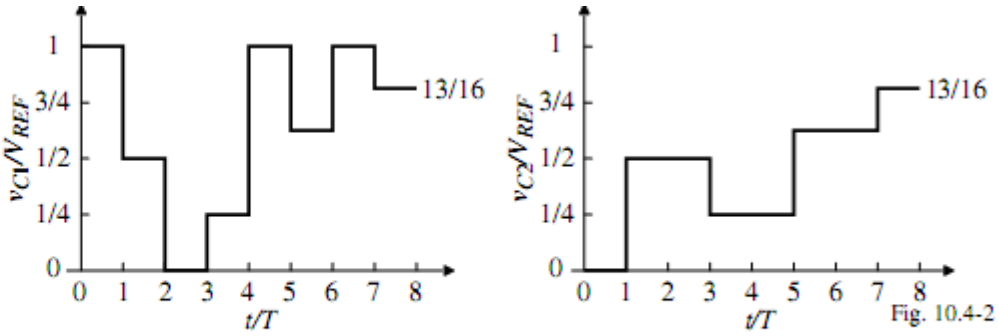


Fig. 10.4-2

Solution

1.) S_4 closes setting $v_{C2} = 0$.
2.) $b_3 = 1$, closes switch S_2 causing $v_{C1} = V_{REF}$.
3.) Switch S_1 is closed causing $v_{C1} = v_{C2} = 0.5V_{REF}$.
4.) $b_2 = 0$, closes switch S_3, causing $v_{C1} = 0\text{V}$.
5.) S_1 closes, the voltage across both C_1 and C_2 is $0.25V_{REF}$.
6.) $b_1 = 1$, closes switch S_2 causing $v_{C1} = V_{REF}$.
7.) S_1 closes, the voltage across both C_1 and C_2 is $(1+0.25)/2V_{REF} = 0.625V_{REF}$.
8.) $b_0 = 1$, closes switch S_2 causing $v_{C1} = V_{REF}$.
9.) S_1 closes, the voltage across both C_1 and C_2 is $(0.625 + 1)/2V_{REF} = 0.8125V_{REF} = (13/16)V_{REF}$.