Low noise amplifier (LNA)

Chapter Outline

Basic LNA Topologies

- ✓ CS Stage with Inductive Load
- ✓ CS Stage with Resistive Feedback
- ✓ CG Stage
- ✓ CS Stage with Inductive Degeneration

Alternative LNA Topologies

- ✓ Variants of CS LNA
- ✓ Noise-Cancelling LNAs
- ✓ Differential LNAs

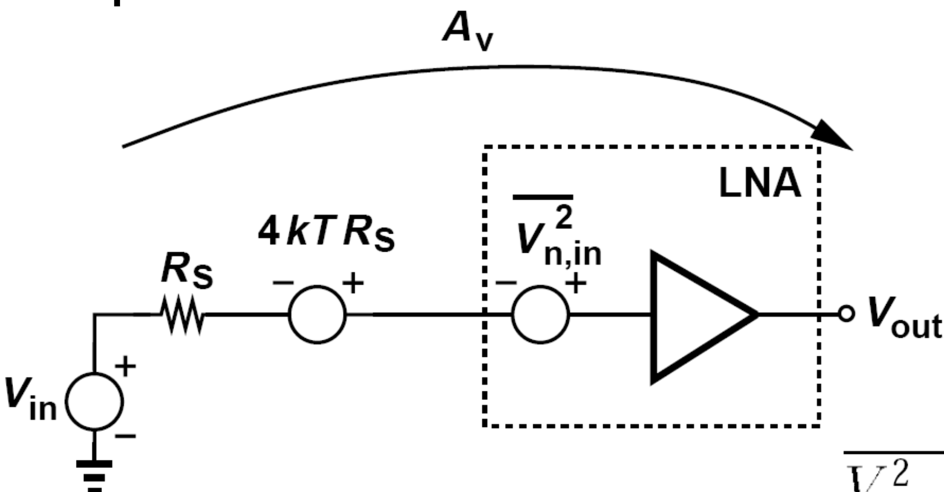
Nonlinearity of LNAs

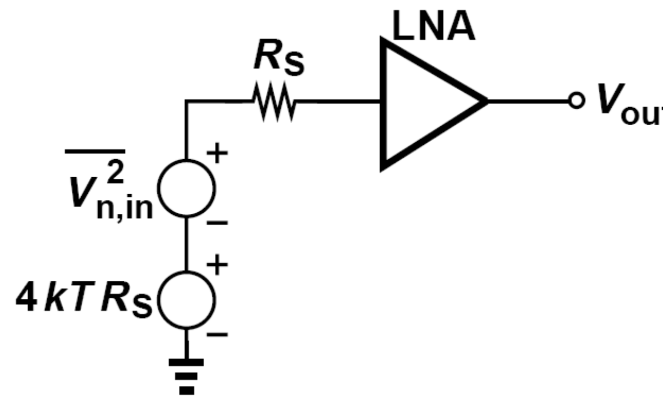
- ✓ Nonlinearity Calculations
- ✓ Differential and Quasi-Differential LNAs

General Considerations: Noise Figure

- **The noise figure of the LNA directly adds to that of the receiver.**

It is expected that the LNA contributes 2 to 3 dB of noise figure. Consider the simple example shown below:





$$\begin{aligned} NF &= \frac{\overline{V^2_{n,out}}}{A_v^2}\cdot\frac{1}{4kTR_S} \\ &= 1+\frac{\overline{V^2_{n,in}}}{4kTR_S}. \end{aligned}$$

A noise figure of 2 dB with respect to a source impedance of 50Ω translates to:

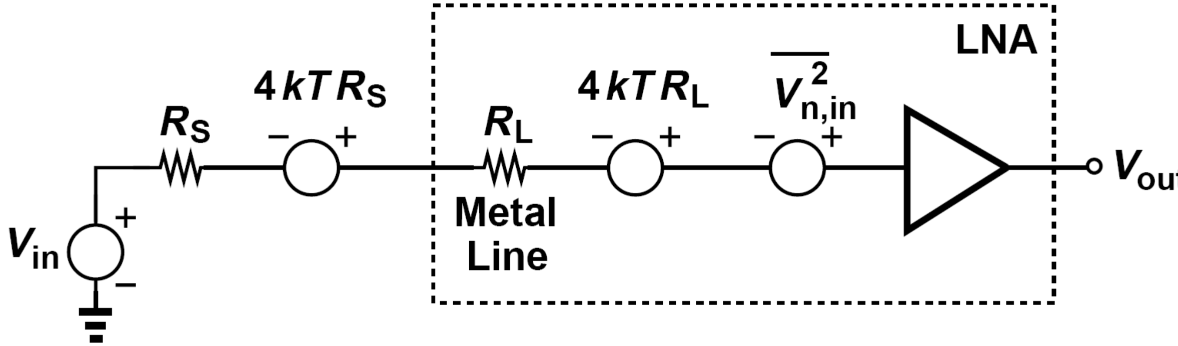
$$\sqrt{\overline{V^2_{n,in}}} = 0.696\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$$ **an extremely low value.**

Example of Metal Resistance and Noise Figure

A student lays out an LNA and connects its input to a pad through a metal line 200 μm long. In order to minimize the input capacitance, the student chooses a width of 0.5 μm for the line. Assuming a noise figure of 2 dB for the LNA and a sheet resistance of 40 mΩ/ □ for the metal line, determine the overall noise figure. Neglect the input-referred noise current of the LNA.

We draw the equivalent circuit as shown in figure below, pretending that the line resistance, R_L, is part of the LNA. The total input-referred noise voltage of the circuit inside the box is therefore equal to $\overline{V_{n,in}^2} + 4kTR_L$. We thus write

$$\begin{aligned} NF_{tot} &= 1 + \frac{\overline{V_{n,in}^2} + 4kTR_L}{4kTR_S} \\ &= 1 + \frac{\overline{V_{n,in}^2}}{4kTR_S} + \frac{R_L}{R_S} \\ &= NF_{LNA} + \frac{R_L}{R_S}, \end{aligned}$$



where NF_{LNA} denotes the noise figure of the LNA without the line resistance. Since NF_{LNA} = 2 dB ≡ 1.58 and R_L = (200/0.5) × 40 mΩ/□ = 16 Ω, we have

$$NF_{tot} = 2.79\,\text{dB}$$

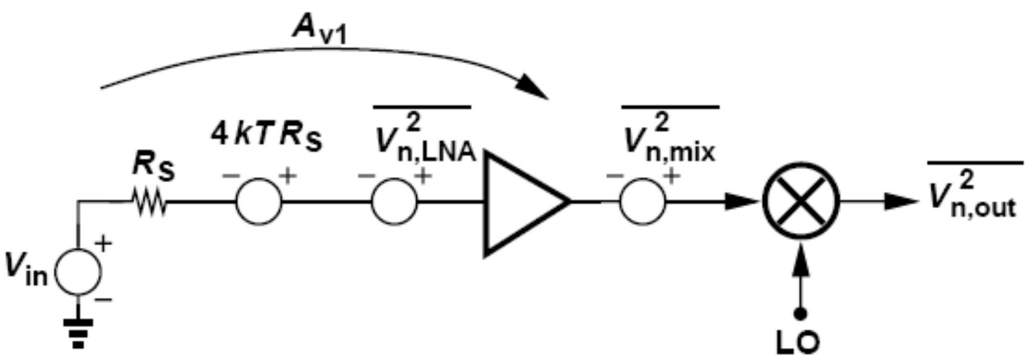
General Considerations: Gain

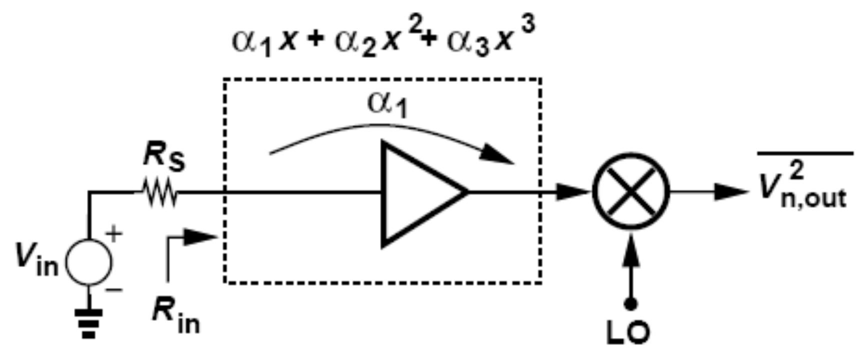
- **The gain of the LNA must be large enough to minimize the noise contribution of subsequent stages, specifically, the downconversion mixer(s).**

The noise and IP_3 of the stage following the LNA are divided by different LNA gains. Assuming a unity voltage gain for the mixer for simplicity, The overall noise figure is thus equal to

$$\mathrm{NF_{tot}} = \frac{A_{v1}^2(\overline{V_{n,LNA}^2} + 4kTR_S) + \overline{V_{n,mix}^2}}{A_{v1}^2} \frac{1}{4kTR_S}$$

$$= \mathrm{NF_{LNA}} + \frac{\overline{V_{n,mix}^2}}{A_{v1}^2} \cdot \frac{1}{4kTR_S}.$$





In figure above (right),

$$\frac{1}{\mathrm{IP}_{3,\mathrm{tot}}^2} = \frac{1}{\mathrm{IP}_{3,\mathrm{LNA}}^2} + \frac{\alpha_1^2}{\mathrm{IP}_{3,\mathrm{mixer}}^2}$$

General Considerations: Input Return Loss

- **The quality of the input match is expressed by the input "return loss," defined as the reflected power divided by the incident power. For a source impedance of R_S, the return loss is given by:**

$$\Gamma = \left| \frac{Z_{in} - R_S}{Z_{in} + R_S} \right|^2$$

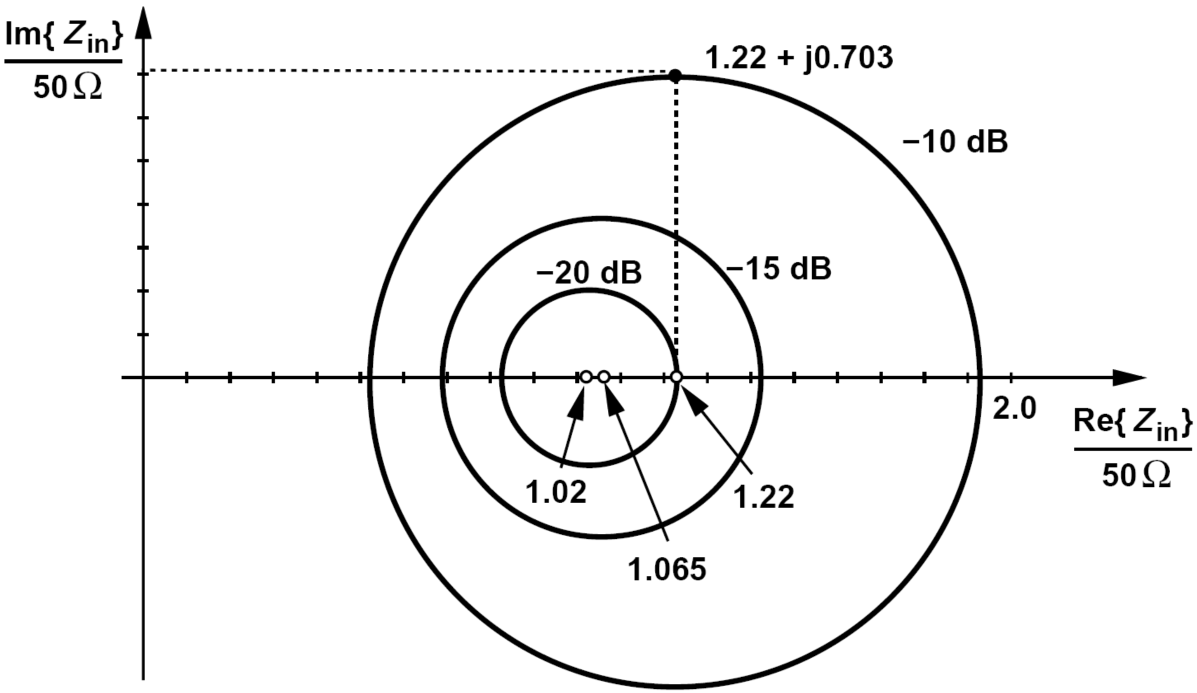


Figure above plots contours of constant Γ in the Z_{in} plane. Each contour is a circle with its center shown.

General Considerations: Stability

- A parameter often used to characterize the stability of circuits is the "Stern stability factor," defined as:

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|}$$

A cascade stage exhibits a high reverse isolation, i.e., $S_{12} \approx 0$. If the output impedance is relatively high so that $S_{22} \approx 1$, determine the stability conditions.

With $S_{12} \approx 0$ and $S_{22} \approx 1$,

$$K \approx \frac{1 - |S_{22}|^2}{2|S_{21}||S_{12}|} > 1$$

and hence

$$|S_{21}| < \frac{1 - |S_{22}|^2}{2|S_{12}|}$$

In other words, the forward gain must not exceed a certain value. For $\Delta < 1$, we have

$$S_{11} < 1$$

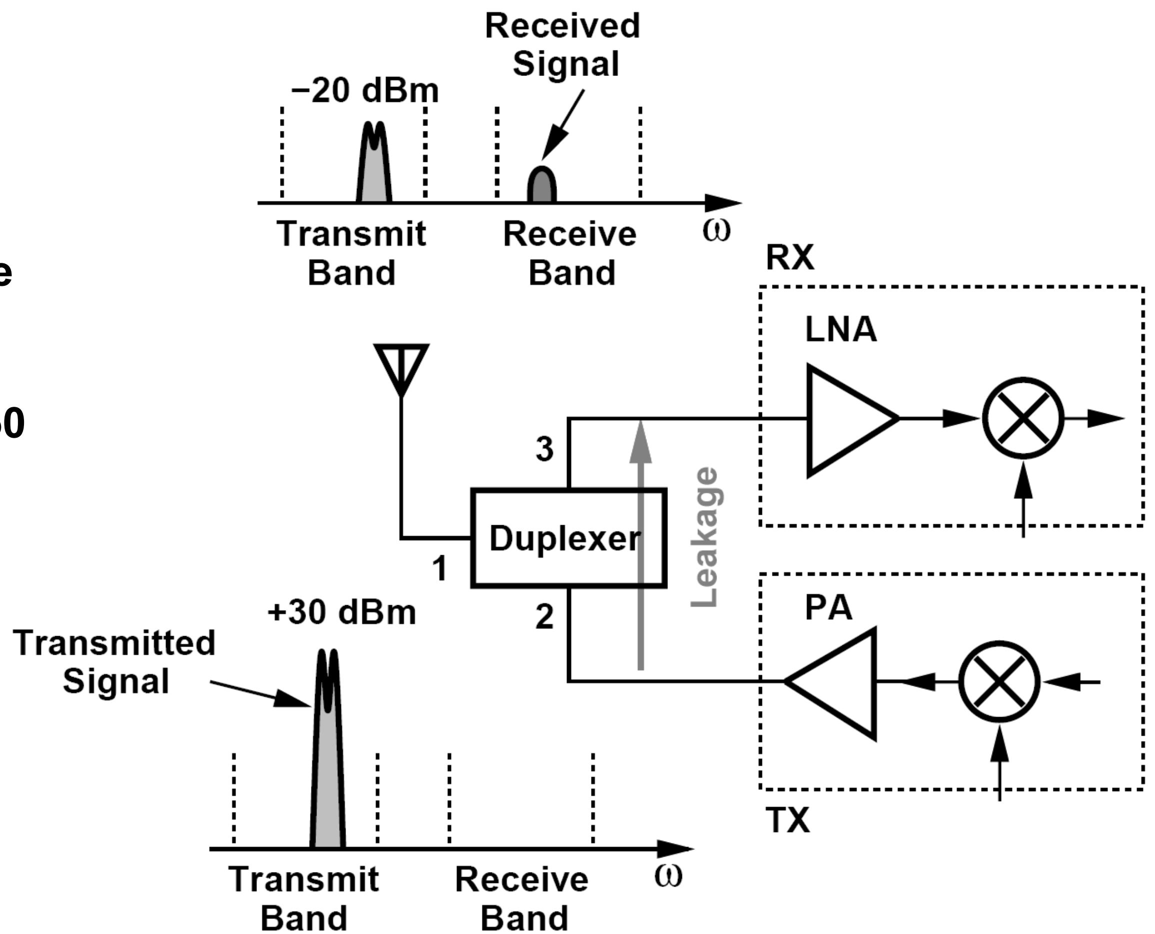
concluding that the input resistance must remain positive.

General Considerations: Linearity

➢ **In most applications, the LNA does not limit the linearity of the receiver.**

An exception to the above rule arises in "full-duplex" systems:

Leakages through the filter and the package yield a finite isolation between ports 2 and 3 as characterized by an S_{32} of about -50 dB. The received signal may be overwhelmed.

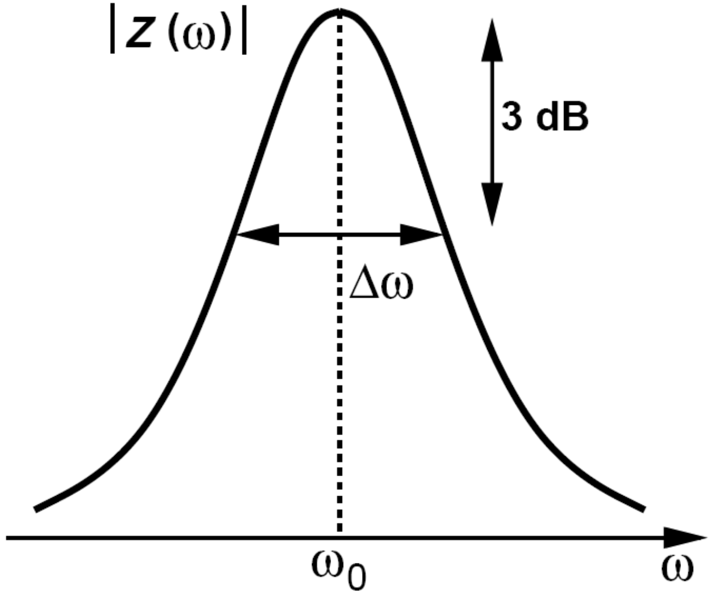


General Considerations: Bandwidth

- The LNA must provide a relatively flat response for the frequency range of interest, preferably with less than 1 dB of gain variation. The LNA -3-dB bandwidth must therefore be substantially larger than the actual band so that the roll-off at the edges remains below 1 dB.

An 802.11a LNA must achieve a -3-dB bandwidth from 5 GHz to 6 GHz. If the LNA incorporates a second-order *LC* tank as its load, what is the maximum allowable tank *Q*?

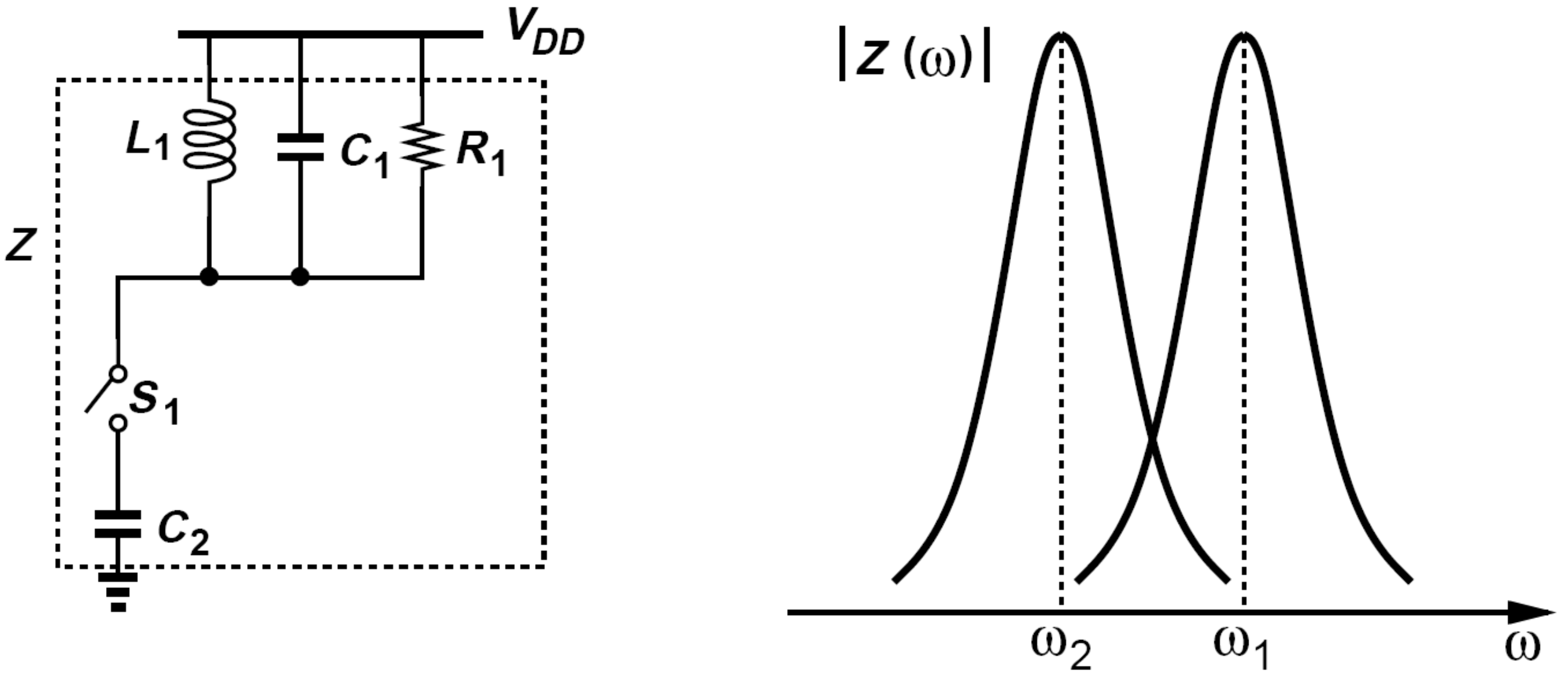
As illustrated in figure below, the fractional bandwidth of an *LC* tank is equal to $\Delta\omega/\omega_0 = 1/Q$. Thus, the *Q* of the tank must remain less than 5.5 GHz/1 GHz = 5.5.



Band Switching

- **LNA designs that must achieve a relatively large fractional bandwidth may employ a mechanism to switch the center frequency of operation.**

As depicted below, an additional capacitor, C_2, can be switched into the tank, thereby changing the center frequency



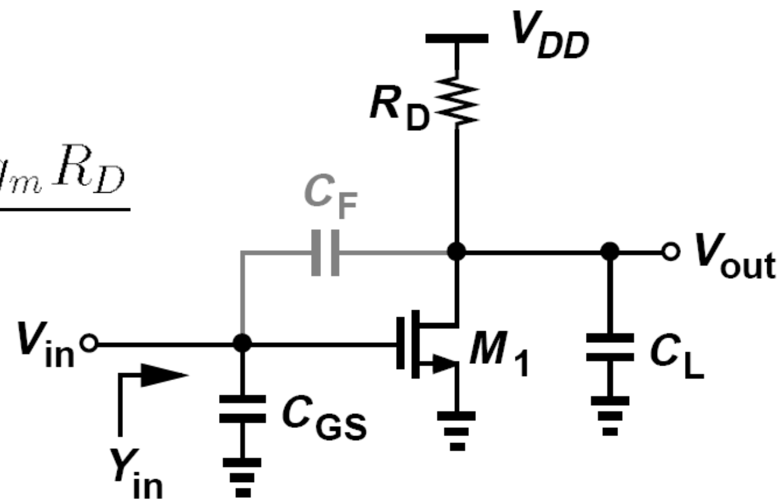
Problem of Input Matching: Input Admittance of a CS Stage

- **LNAs are typically designed to provide a 50-W input resistance and negligible input reactance. This requirement limits the choice of LNA topologies.**

The real and imaginary parts of the input admittance are, respectively, equal to:

$$Re\{Y_{in}\} = R_D C_F \omega^2 \frac{C_F + g_m R_D (C_L + C_F)}{R_D^2 (C_L + C_F)^2 \omega^2 + 1}$$

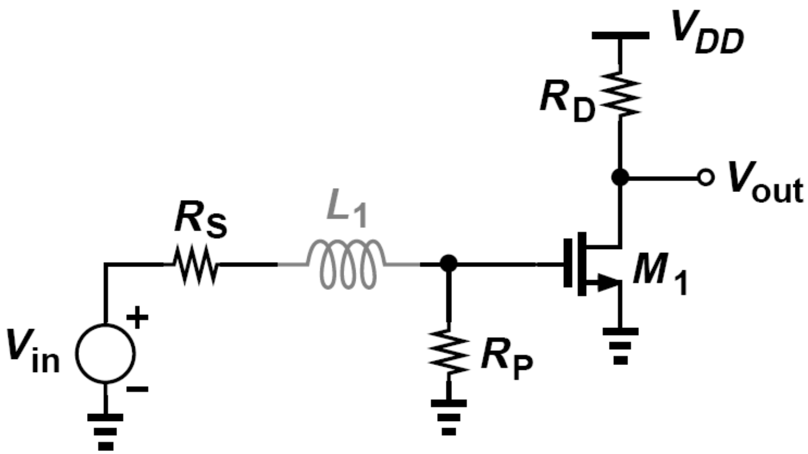
$$Im\{Y_{in}\} = C_F \omega \frac{R_D^2 C_L (C_L + C_F) \omega^2 + 1 + g_m R_D}{R_D^2 (C_L + C_F)^2 \omega^2 + 1}$$

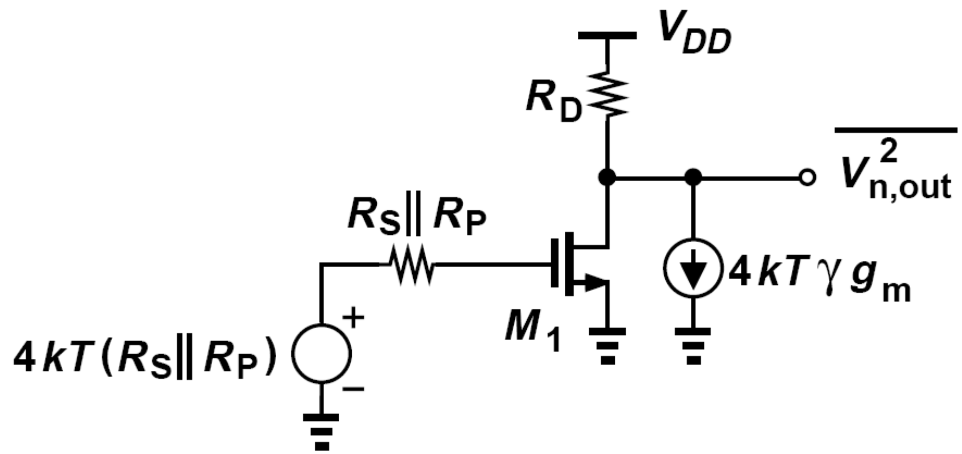


Why did we compute the input admittance rather than the input impedance for the circuit of figure above.

The choice of one over that other is somewhat arbitrary. In some circuits, it is simpler to compute Y_{in}. Also, if the input capacitance is cancelled by a parallel inductor, then $Im\{Y_{in}\}$ is more relevant. Similarly, a series inductor would cancel $Im\{Z_{in}\}$. We return to these concepts later in this chapter.

Resistive Termination for Matching





- **Such a topology is designed in three steps:**

  (1) M_1 and R_D provide the required noise figure and gain

  (2) R_P is placed in parallel with the input to provide $Re\{Z_{in}\} = 50\Omega$

  (3) an inductor is interposed between R_S and the input to cancel $Im\{Z_{in}\}$.

express the total output noise as:

$$\overline{V_{n,out}^2} = 4kT(R_S||R_P)(g_m R_D)^2 + 4kT\gamma g_m R_D^2 + 4kT R_D$$

the noise figure is given by:

$$\mathrm{NF} = 1 + \frac{R_S}{R_P} + \frac{\gamma R_S}{g_m (R_S||R_P)^2} + \frac{R_S}{g_m^2 (R_S||R_P)^2 R_D}$$

Example of Input Matching by Transforming a Large Resistance Down (Ⅰ)

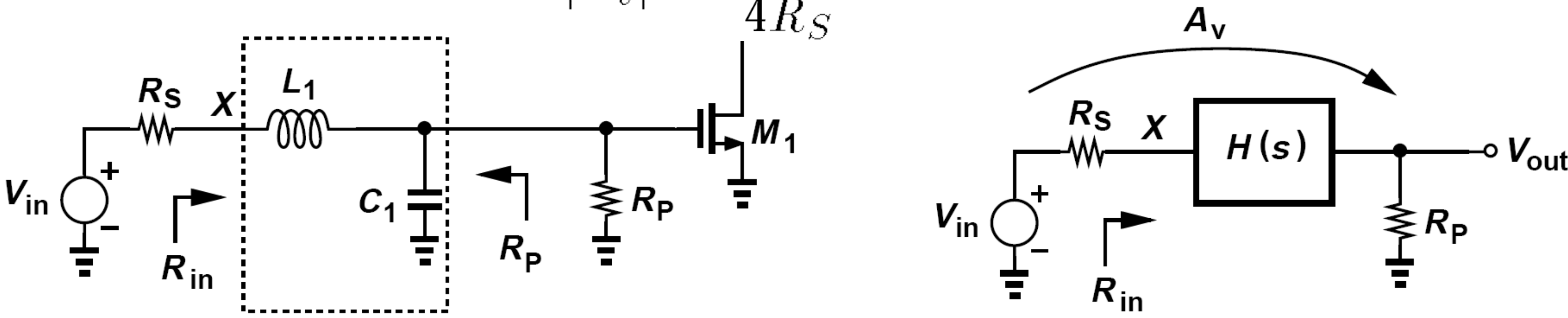
A student decides to defy the above observation by choosing a large R_P and transforming its value down to R_S. The resulting circuit is shown below (left), where C_1 represents the input capacitance of M_1. (The input resistance of M_1 is neglected.) Can this topology achieve a noise figure less than 3 dB?

Consider the more general circuit in figure below (right), where *H(s)* represents a lossless network similar to L_1 and C_1. Since it is desired that $Z_{in} = R_S$, the power delivered by V_{in} to the input port of *H(s)* is equal to $(V_{in,rms}/2)^2/R_S$. This power must also be delivered to R_P :

$$\frac{V_{in,rms}^2}{4R_S} = \frac{V_{out,rms}^2}{R_P}$$

It follows that

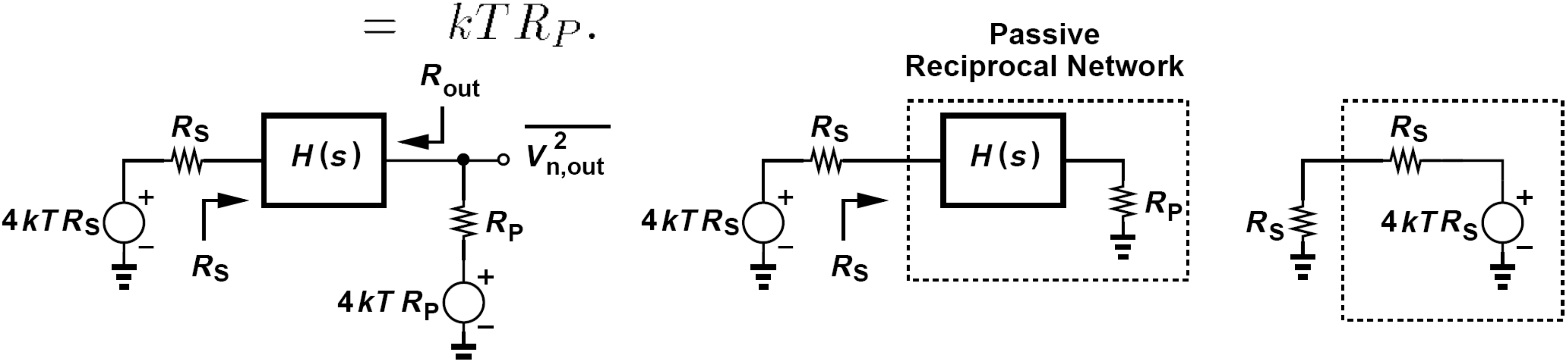
$$|A_v|^2 = \frac{R_P}{4R_S}$$



Example of Input Matching by Transforming a Large Resistance Down (Ⅱ)

Let us now compute the output noise with the aid of figure below (left). The output noise due to the noise of R_S is readily obtained

$$\overline{V_{n,out}^2}|_{RS} = 4kTR_S \cdot \frac{R_P}{4R_S} = kTR_P.$$



How about the noise of R_P? We must first determine the value of R_{out}. We draw the circuit as depicted above (middle) and recall that a passive reciprocal network exhibiting a real port impedance of R_S also produces a thermal noise of $4kTR_S$. From the equivalent circuit shown above (right), we note that the noise power delivered to the R_S on the left is equal to kT.

$$4kTR_P\left(\frac{R_{out}}{R_{out}+R_P}\right)^2 \cdot \frac{1}{R_{out}} = kT \quad \Rightarrow \quad R_{out} = R_P$$

$$\overline{V_{n,out}^2}|_{RP} = kTR_P \quad \Rightarrow \quad \mathrm{NF} = 2$$

LNA Topologies: Overview

➢ **Our preliminary studies thus far suggest that the noise figure, input matching, and gain constitute the principal targets in LNA design. We present a number of LNA topologies and analyze their behavior with respect to these targets.**

Common−Source Stage with	Common−Gate Stage with	Broadband Topologies
• Inductive Load • Resistive Feedback • Cascode, Inductive Load, Inductive Degeneration	• Inductive Load • Feedback • Feedforward • Cascode and Inductive Load	• Noise−Canceling LNAs • Reactance−Canceling LNAs

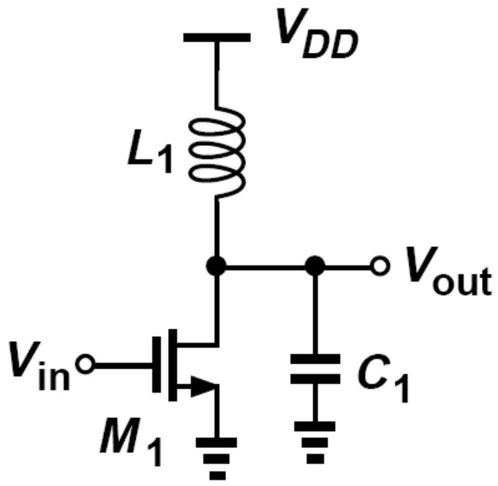
Common-Source Stage with Inductive Load

In general, the trade-off between the voltage gain and the supply voltage in the *CS stage with resistive load* makes it less attractive as the latter scales down with technology. For example, at low frequencies,

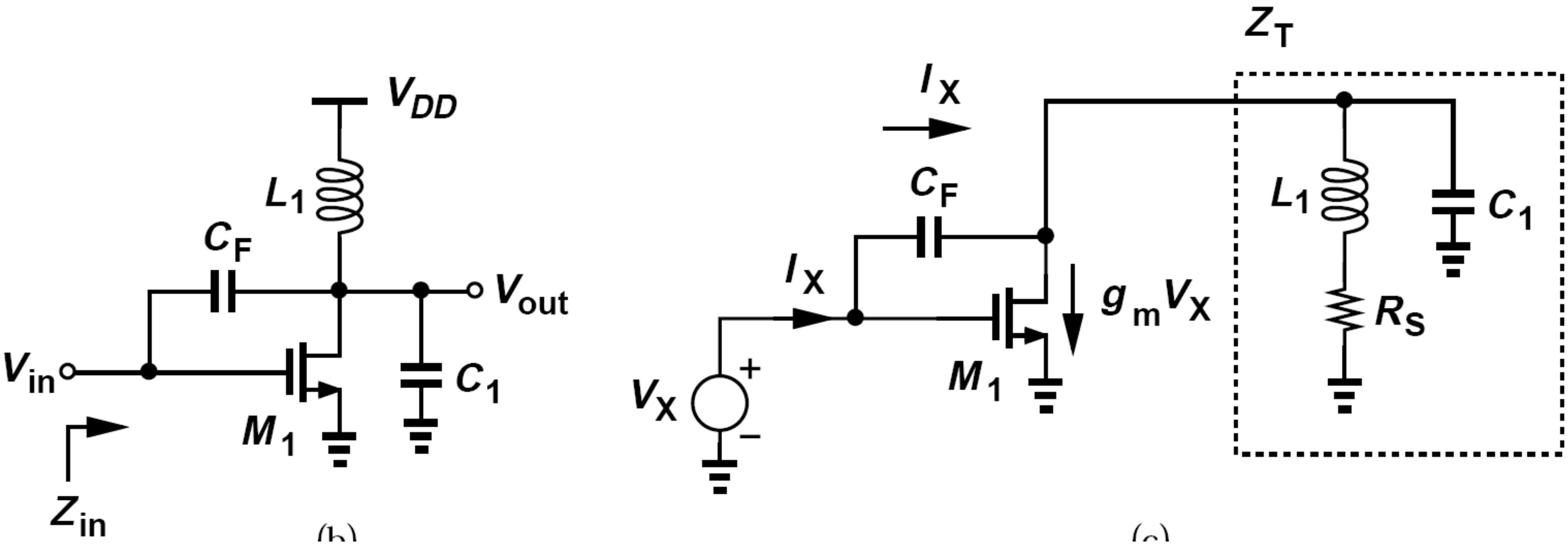
$$\begin{aligned} |A_v| &= g_m R_D \\ &= \frac{2I_D}{V_{GS}-V_{TH}} \cdot \frac{V_{RD}}{I_D} \\ &= \frac{2V_{RD}}{V_{GS}-V_{TH}}, \end{aligned}$$

To circumvent the trade-off expressed above and also operate at higher frequencies, the CS stage can incorporate an inductive load.

- **Can operate with very low supply voltages**
- **L_1 resonates with the total capacitance at the output node, affording a much higher operation frequency than does the resistively-loaded counterpart**



Input Matching of CS Stage with Inductive Load（Ⅰ）



We redraw the circuit as depicted above (right) the inductor loss is modeled by a series resistance, R_S, The tank impedance is given by

$$Z_T = \frac{L_1 s + R_S}{L_1 C_1 s^2 + R_S C_1 s + 1}$$

Adding the voltage drop across C_F to the tank voltage, we have

$$V_X = \frac{I_X}{C_F s} + (I_X - g_m V_X) Z_T$$

Input Matching of CS Stage with Inductive Load (Ⅱ)

Substitution of Z_T gives:

$$Z_{in}(s) = \frac{V_X}{I_X} = \frac{L_1(C_1 + C_F)s^2 + R_S(C_1 + C_F)s + 1}{[L_1C_1s^2 + (R_SC_1 + g_mL_1)s + 1 + g_mR_S]C_Fs}$$

For $s = j\omega$: $$Z_{in}(j\omega) = \frac{1 - L_1(C_1 + C_F)\omega^2 + jR_S(C_1 + C_F)\omega}{[-(R_SC_1 + g_mL_1)\omega + j(g_mR_S - L_1C_1\omega^2 + 1)]C_F\omega}.$$

Since the real part of a complex fraction (*a*+*jb*)/(*c*+*jd*) is equal to (*ac*+*bd*)/(c^2 +d^2), we have

$$Re\{Z_{in}\} = \frac{[1 - L_1(C_1 + C_F)\omega^2][-(R_SC_1 + g_mL_1)\omega] + R_S(C_1 + C_F)(g_mR_S - L_1C_1\omega^2 + 1)\omega^2}{D}$$

It is thus possible to select the values so as to obtain $Re\{Z_{in}\}$ = 50Ω

Neutralization of C_F by L_F

The feedback capacitance gives rise to a negative input resistance at other frequencies, potentially causing instability.

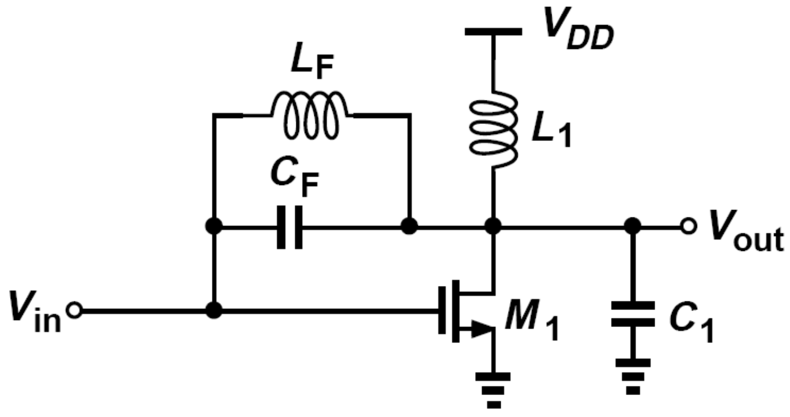
$$Re\{Z_{in}\} = \frac{g_m L_1^2 (C_1 + C_F)\omega^2 + R_S(1 + g_m R_S)(C_1 + C_F) - (R_S C_1 + g_m L_1)}{D}\omega$$

The numerator falls to zero at a frequency given by

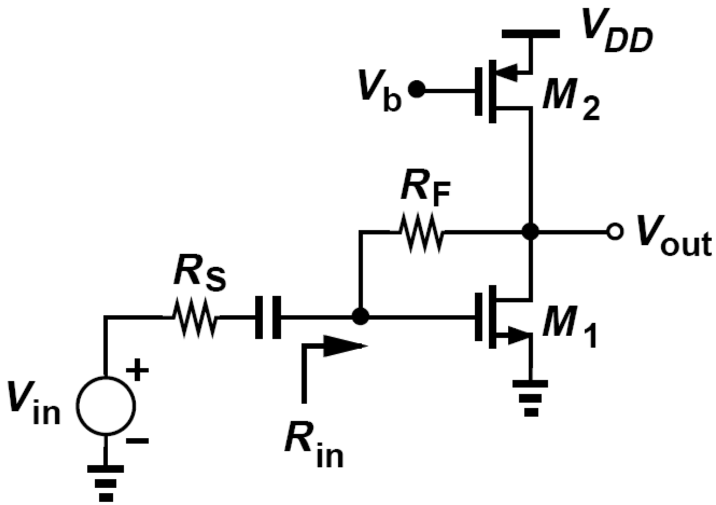
$$\omega_1^2 = \frac{R_S C_1 + g_m L_1 - (1 + g_m R_S) R_S (C_1 + C_F)}{g_m L_1^2 (C_1 + C_F)}$$

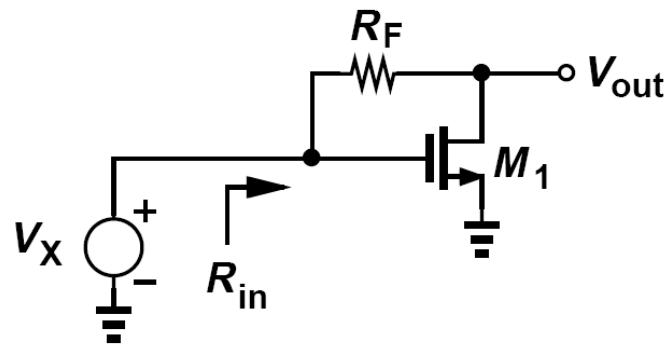
Thus, at this frequency (if it exists), *$Re\{Z_{in}\}$* changes sign.

- **It is possible to "neutralize" the effect of C_F in some frequency range through the use of parallel resonance.**
- **Will introduce significant parasitic capacitances at the input and output and degrading the performance.**



Common-Source Stage with Resistive Feedback





If channel-length modulation is neglected, we have: $R_{in} = \frac{1}{g_{m1}}$

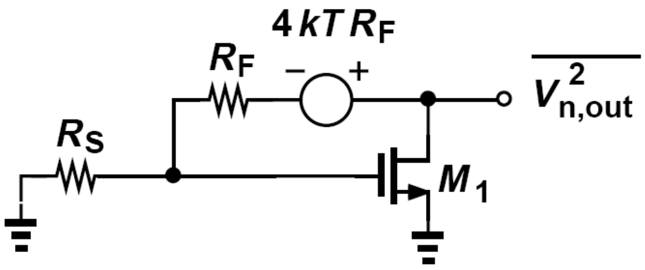
We must choose: $g_{m1} = \frac{1}{R_S}$

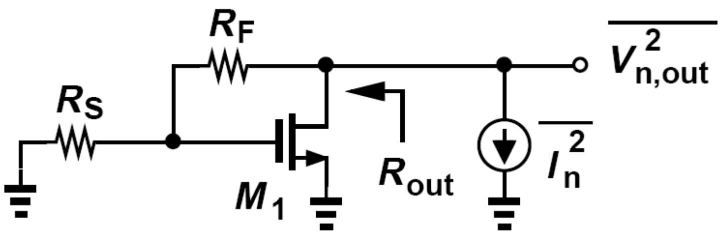
In figure above (right): $V_X - g_{m1} V_X R_F = V_{out}$

$$\frac{V_{out}}{V_X} = 1 - g_{m1} R_F = 1 - \frac{R_F}{R_S}.$$

$$A_v = \frac{1}{2}\left(1 - \frac{R_F}{R_S}\right) \approx -\frac{R_F}{R_S}.$$

Noise Figure of CS Stage with Resistive Feedback





The noise of RF appears at the output:

$$\overline{V_{n,out}^2}|_{RF} = 4kTR_F$$

$$R_{out} = \left[\frac{1}{g_{m1}}\left(1+\frac{R_F}{R_S}\right)\right]||(R_F+R_S)$$

$$= \frac{1}{2}(R_F+R_S).$$

$$\overline{V_{n,out}^2}|_{M1,M2} = 4kT\gamma(g_{m1}+g_{m2})\frac{(R_F+R_S)^2}{4}$$

$$NF = 1+\frac{4R_F}{R_S\left(1-\frac{R_F}{R_S}\right)^2}+\frac{\gamma(g_{m1}+g_{m2})(R_F+R_S)^2}{\left(1-\frac{R_F}{R_S}\right)^2 R_S}$$

$$\approx 1+\frac{4R_S}{R_F}+\gamma(g_{m1}+g_{m2})R_S$$

$$\approx 1+\frac{4R_S}{R_F}+\gamma+\gamma g_{m2}R_S.$$

Example of NF and Transistor Overdrive Voltages

Express the fourth term on the right-hand side of Noise Figure calculated above in terms of transistor overdrive voltages.

Solution:

Since $g_m = 2I_D/(V_{GS} - V_{TH})$, we write $g_{m2}R_S = g_{m2}/g_{m1}$ and

$$\frac{g_{m2}}{g_{m1}} = \frac{(V_{GS} - V_{TH})_1}{|V_{GS} - V_{TH}|_2}$$

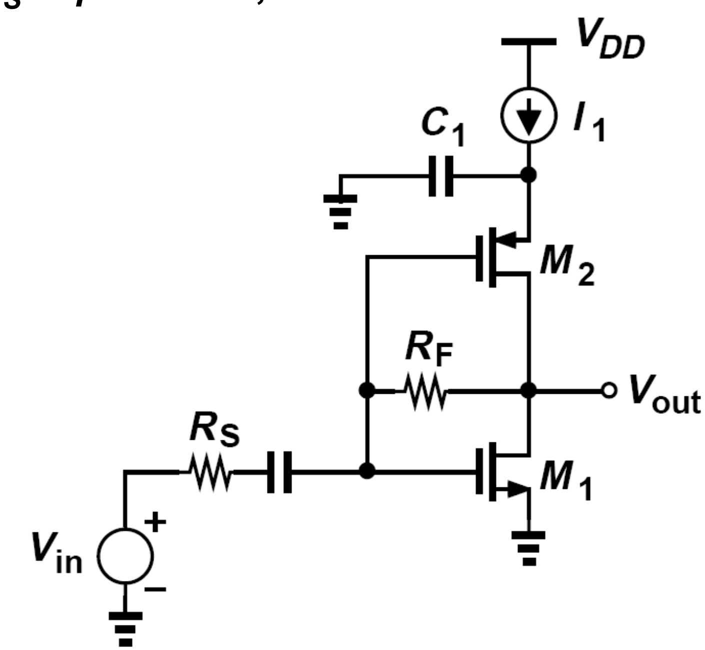
That is, the fourth term becomes negligible only if the overdrive of the current source remains much higher than that of M_1—a difficult condition to meet at low supply voltages because $|V_{DS2}| = V_{DD} - V_{GS1}$. We should also remark that heavily velocity-saturated MOSFETs have a transconductance given by $g_m = I_D/(V_{GS} - V_{TH})$ and still satisfy equation above.

Example of CS Stage with Active Load

In the circuit of figure below, the PMOS current source is converted to an "active load," amplifying the input signal. The idea is that, if M_2 amplifies the input in addition to injecting noise to the output, then the noise figure may be lower. Neglecting channel-length modulation, calculate the noise figure. (Current source I_1 defines the bias current and C_1 establishes an ac ground at the source of M_2).

For small-signal operation, M_1 and M_2 appear in parallel, behaving as a single transistor with a transconductance of $g_{m1} + g_{m2}$. Thus, for input matching, $g_{m1} + g_{m2} = 1/R_S$. The noise figure is still given by previous equation, except that $(g_{m1} + g_{m2})R_S = \gamma$. That is,

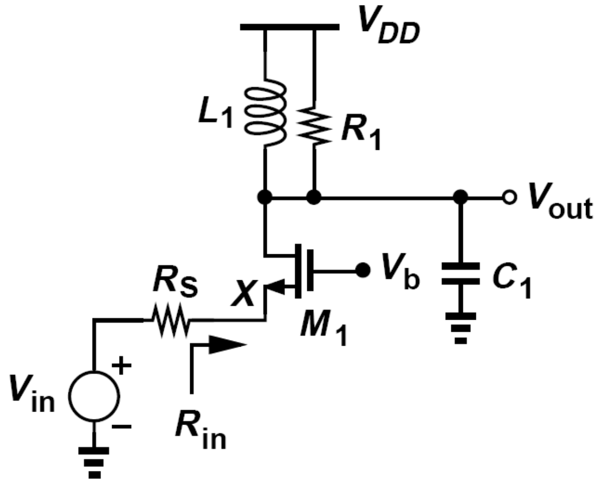
$$\mathrm{NF} \approx 1 + \frac{4R_S}{R_F} + \gamma$$

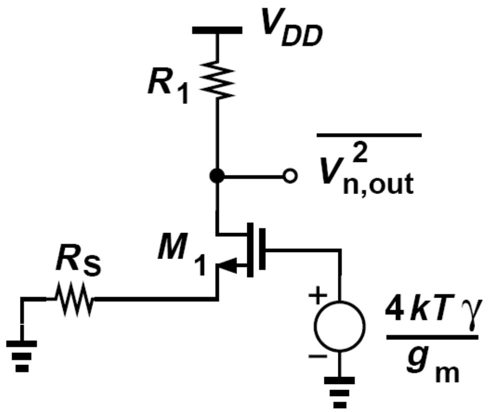


This circuit is therefore superior, but it requires a supply voltage equal to $V_{GS1} + |V_{GS2}| + V_{I1}$, where V_{I1} denotes the voltage headroom necessary for I_1.

Common-Gate Stage

- The low input impedance of the common-gate (CG) stage makes it attractive for LNA design.





The voltage gain from *X* to the output node at the output resonance frequency is then equal to:

$$\frac{V_{out}}{V_X} = g_m R_1 = \frac{R_1}{R_S}$$

And noise:

$$\overline{V^2_{n,out}}|_{M1} = \frac{4kT\gamma}{g_m}\left(\frac{R_1}{R_S+\frac{1}{g_m}}\right)^2 = kT\gamma\frac{R_1^2}{R_S}.$$

$$\Rightarrow \text{NF} = 1+\frac{\gamma}{g_m R_S}+\frac{R_S}{R_1}\left(1+\frac{1}{g_m R_S}\right)^2 = 1+\gamma+4\frac{R_S}{R_1}.$$

Example of Noise in CG Stage with Different Biasing (Ⅰ)

We wish to provide the bias current of the CG stage by a current source or a resistor. Compare the additional noise in these two cases.

For a given V_{b1} and V_{GS1}, the source voltages of M_1 in the two cases are equal and hence V_{DS2} is equal to the voltage drop across R_B ($=V_{RB}$). Operating in saturation, M_2 requires that $V_{DS2} \geq V_{GS2} - V_{TH2}$. We express the noise current of M_2 as

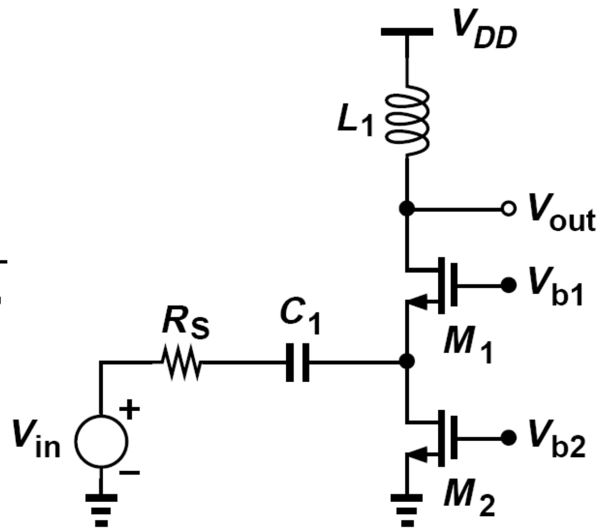
$$\overline{I^2_{n,M2}} = 4kT\gamma g_{m2}$$

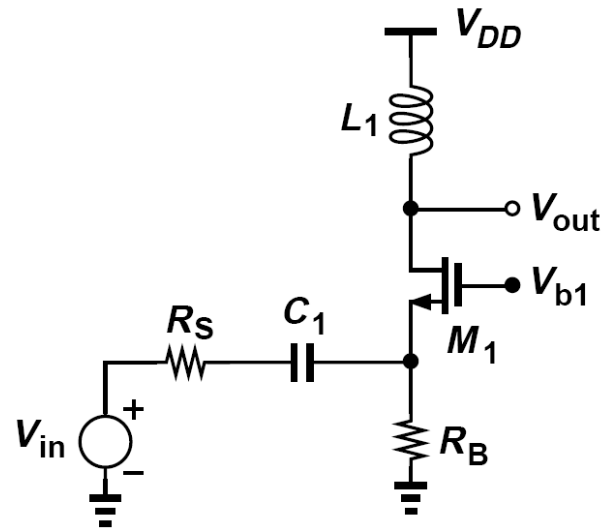
$$= 4kT\gamma \frac{2I_D}{V_{GS2} - V_{TH2}}$$

And that of R_B as

$$\overline{I^2_{n,RB}} = \frac{4kT}{R_B}$$

$$= 4kT \frac{I_D}{V_{RB}}$$



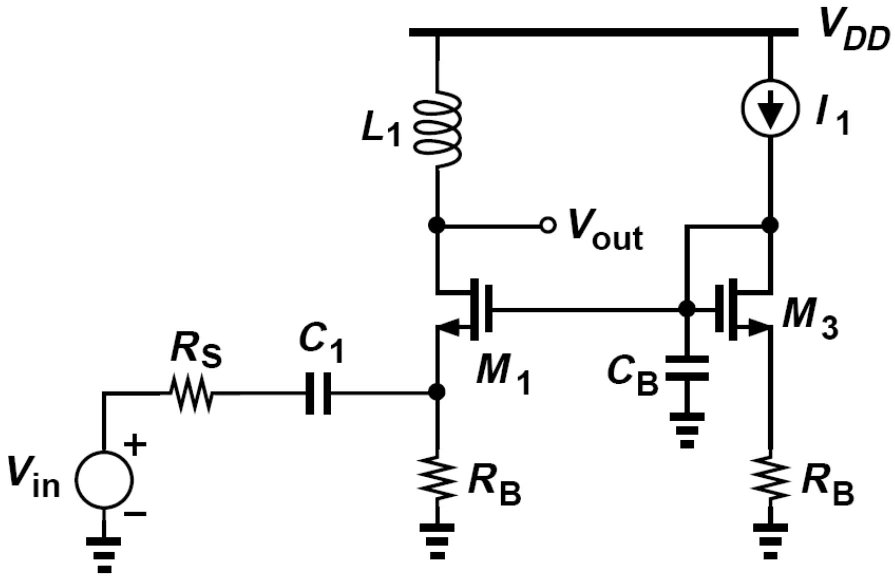


Example of Noise in CG Stage with Different Biasing (Ⅱ)

We wish to provide the bias current of the CG stage by a current source or a resistor. Compare the additional noise in these two cases.

Since V_{GS2}-V_{TH2} ≤ V_{RB}, the noise contribution of M_2 is about twice that of R_B (for $\gamma \approx 1$). Additionally, M_2 may introduce significant capacitance at the input node.

The use of a resistor is therefore preferable, so long as R_B is much greater than R_S so that it does not attenuate the input signal. Note that the input capacitance due to M_1 may still be significant. We will return to this issue later. Figure 5.18 shows an example of proper biasing in this case.

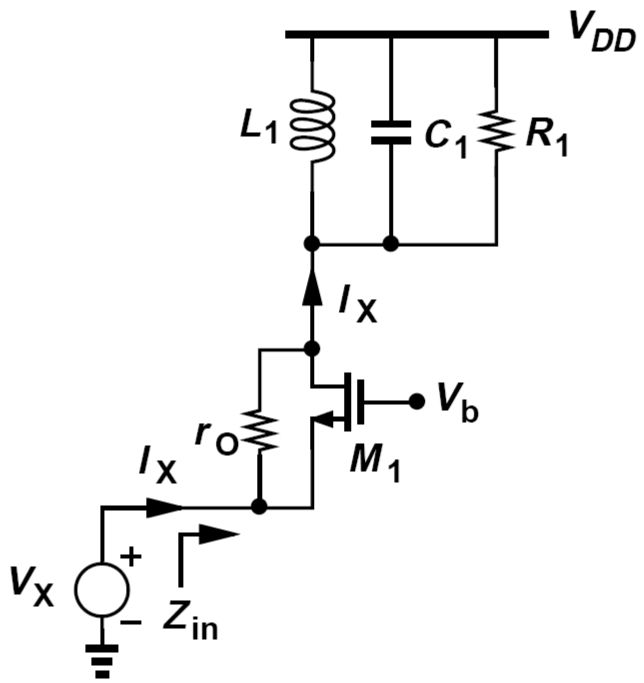


Input Impedance of CG Stage in the Presence of r_O

- **The positive feedback through r_o raises the input impedance**

$$V_X = r_O(I_X - g_m V_X) + I_X R_1$$

$$\frac{V_X}{I_X} = \frac{R_1 + r_O}{1 + g_m r_O}$$



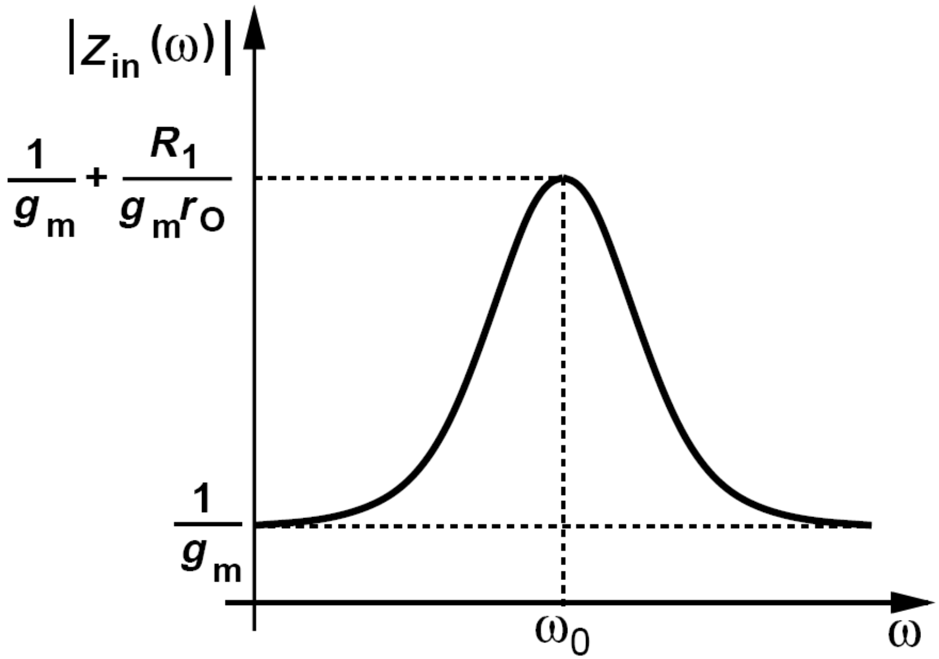
Thus, the term $R_1/(g_m r_O)$ may become comparable with or even exceed the term $1/g_m$, yielding an input resistance substantially higher than 50 Ω

Example of Input Impedance of CG Stage

Neglecting the capacitances of M_1 in figure above, plot the input impedance as a function of frequency.

Solution:

At very low or very high frequencies, the tank assumes a low impedance, yielding $R_{in} = 1/g_m$ [or $1/(g_m + g_{mb})$ if body effect is considered]. Figure below depicts the behavior.



More about Channel-Length Modulation

With the strong effect of R_1 on R_{in}, we must equate the actual input resistance to R_S to guarantee input matching:

$$R_S = \frac{R_1 + r_O}{1 + g_m r_O}$$

The voltage gain of the CG stage with a finite r_O is expressed as

$$\frac{V_{out}}{V_{in}} = \frac{g_m r_O + 1}{r_O + g_m r_O R_S + R_S + R_1} R_1$$

$$\frac{V_{out}}{V_{in}} = \frac{g_m r_O + 1}{2\left(1 + \frac{r_O}{R_1}\right)}$$

If r_O and R_1 are comparable, then the voltage gain is on the order of $g_m r_O$=4, a very low value.

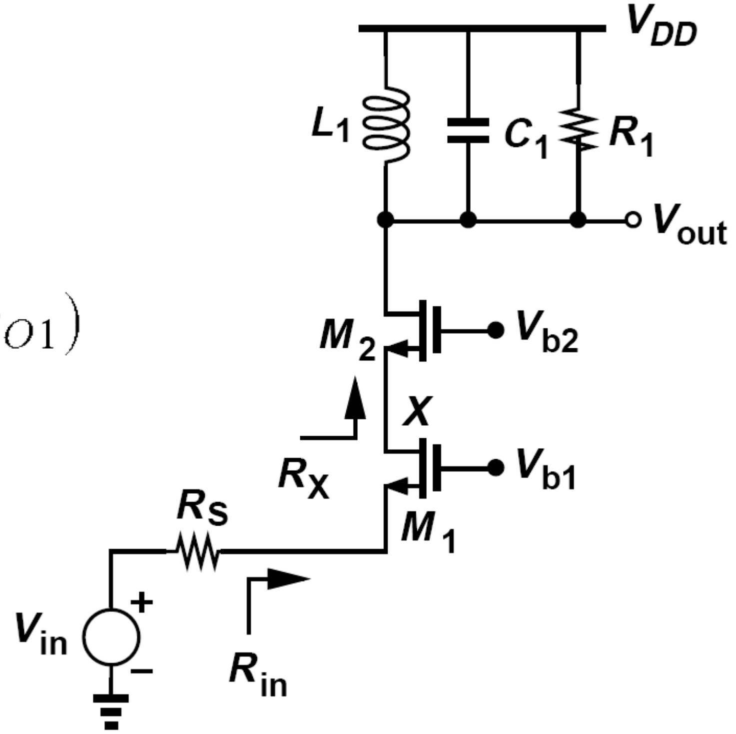
- **In summary, the input impedance of the CG stage is too low if channel-length modulation is neglected and too high if it is not.**
- **In order to alleviate the above issue, the channel length of the transistor can be increased**

Cascode CG Stage

An alternative approach to lowering the input impedance is to incorporate a cascode device

$$R_X = \frac{R_1 + r_{O2}}{1 + g_{m2} r_{O2}}$$

$$R_{in} = \left(\frac{R_1 + r_{O1}}{1 + g_{m2} r_{O2}} + r_{O1}\right) \div (1 + g_{m1} r_{O1})$$

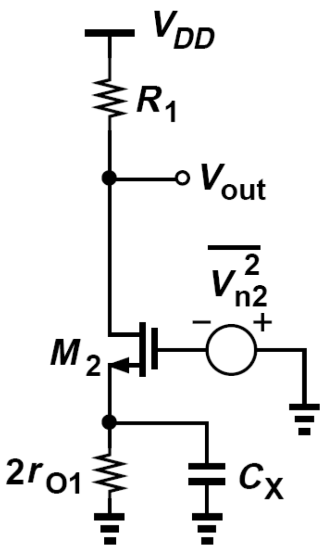


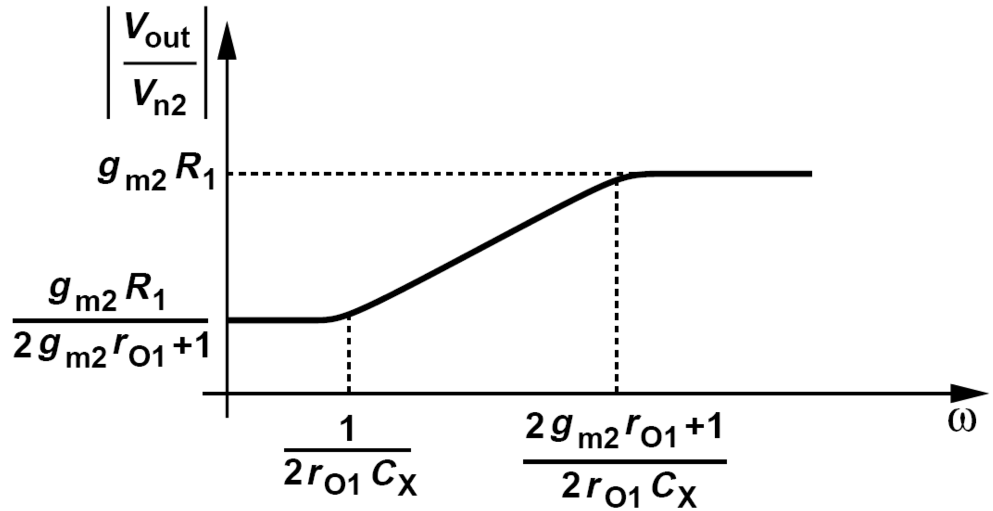
If $g_m r_O$ >>1, then

$$R_{in} \approx \frac{1}{g_{m1}} + \frac{R_1}{g_{m1} r_{O1} g_{m2} r_{O2}} + \frac{1}{g_{m1} r_{O1} g_{m2}}$$

- **R_1 is divided by the product of two intrinsic gains, its effect remains negligible. Similarly, the third term is much less than the first if g_{m1} and g_{m2} are roughly equal. Thus, $R_{in} \approx 1/g_{m1}$.**

Issues of Cascode CG Stage: Noise Contribution of M_2





Neglecting the gate-source capacitance, channel-length modulation, and body effect of M_2, we express the transfer function from V_{n2} to the output at the resonance frequency as

$$\frac{V_{n,out}}{V_{n2}}(s) = \frac{R_1}{\frac{1}{g_{m2}} + (2r_{O1})||\frac{1}{C_X s}}$$

$$= \frac{2r_{O1}C_X s + 1}{2r_{O1}C_X s + 2g_{m2}r_{O1} + 1} g_{m2}R_1$$

The noise contribution of M_2 is negligible for frequencies up to the zero frequency, $(2r_{O1}C_X)^{-1}$, but begins to manifest itself thereafter.

Computation of Gain with C_{GS2}

Assuming $2r_{O1} >> |C_X s|^{-1}$ at frequencies of interest so that the degeneration impedance in the source of M_2 reduces to C_X, recompute the above transfer function while taking C_{GS2} into account. Neglect the effect of r_{O2}.

Writing a KVL in the input loop gives

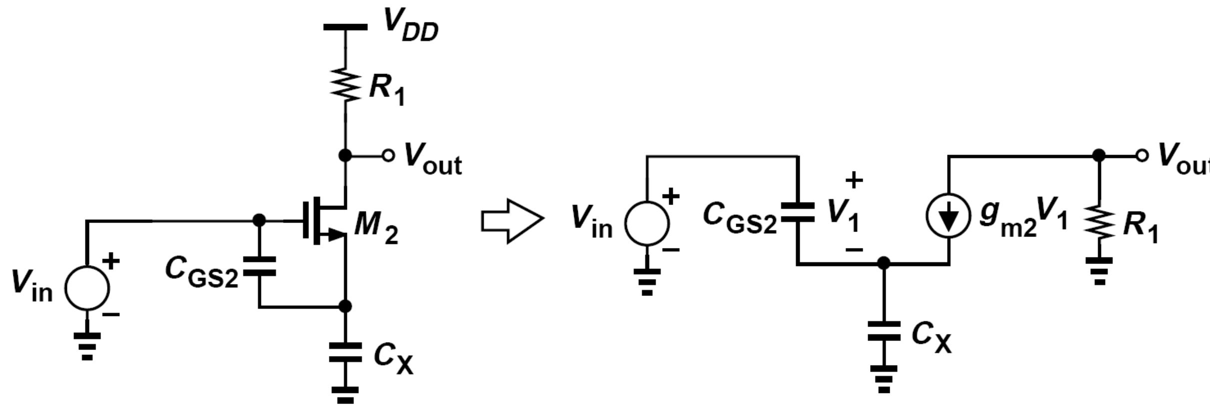
$$\left(-\frac{V_{out}C_{GS2}s}{g_{m2}R_1} - \frac{V_{out}}{R_1}\right)\frac{1}{C_X s} - \frac{V_{out}}{g_{m2}R_1} = V_{in}$$

$$\Rightarrow \frac{V_{out}}{V_{in}} = \frac{-g_{m2}R_1C_X s}{(C_{GS2}+C_X)s + g_{m2}}$$

At frequencies well below the f_T of the transistor

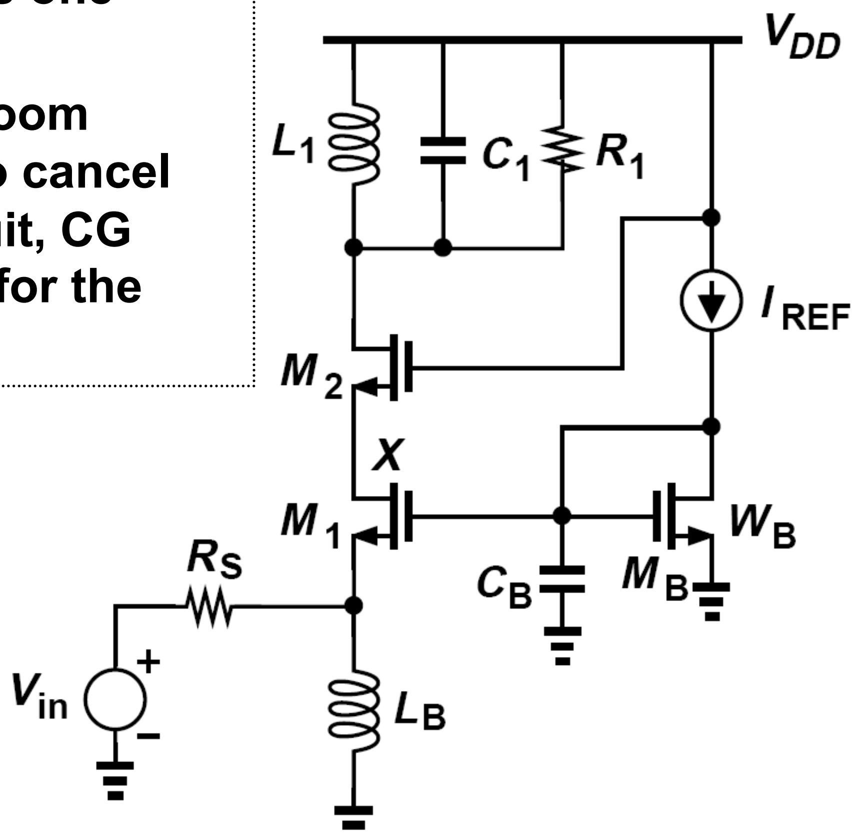
$$\frac{V_{out}}{V_{in}} \approx -R_1 C_X s$$

That is, the noise of M_2 reaches the output unattenuated if ω is much greater than $(2r_{O1}C_X)^{-1}$



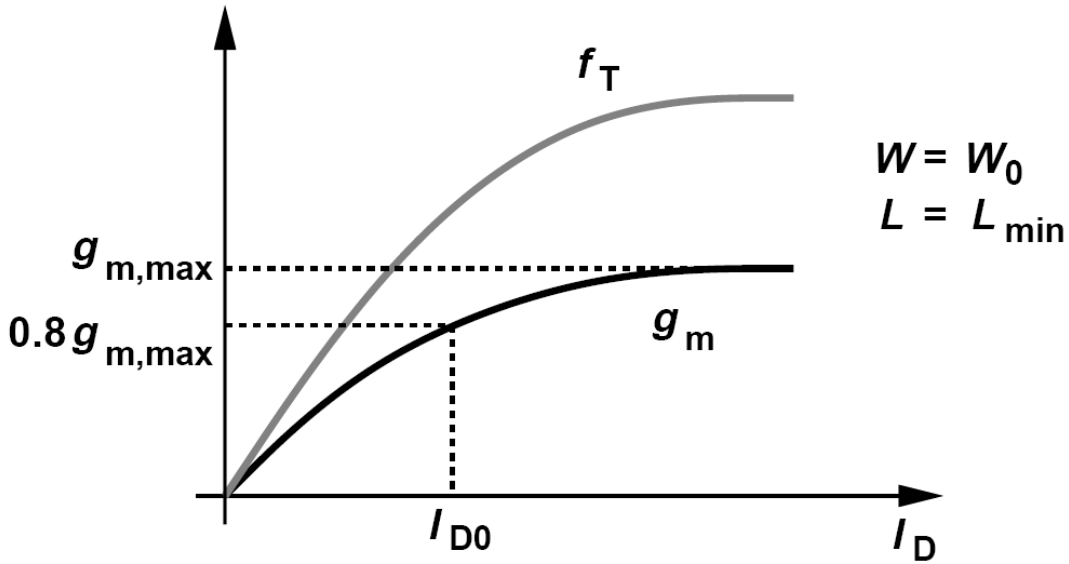
Issues of Cascode CG Stage: Voltage Headroom Limitation

- **The two transistors M_1 and M_2 consume a voltage headroom of one V_{GS} plus one overdrive (V_{GS1} -V_{TH1}).**
- **In order to avoid the noise-headroom trade-off imposed by R_B, and also cancel the input capacitance of the circuit, CG stages often employ an inductor for the bias path.**



Design Procedure (Ⅰ)

➢ **In the first step, the dimensions and bias current of M_1 must be chosen such that a transconductance of $(50\ \Omega)^{-1}$ is obtained.**

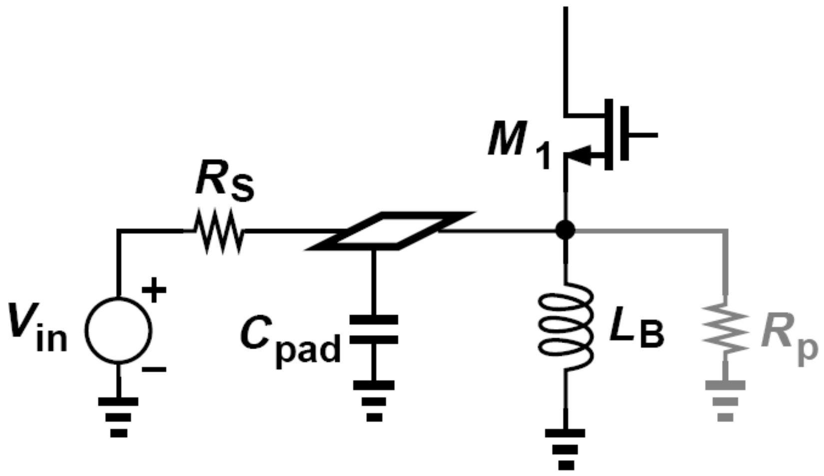


To avoid excessive power consumption, we select a bias current, I_{D0}, that provides 80 to 90% of the saturated g_m.

With W_0 and I_{D0} known, any other value of transconductance can be obtained by simply scaling the two proportionally.

Design Procedure (Ⅱ)

- In the second step, we compute the necessary value of L_B



Thus, L_B must resonate with C_{pad} + C_{SB1} + C_{GS1} and its own capacitance at the frequency of interest.

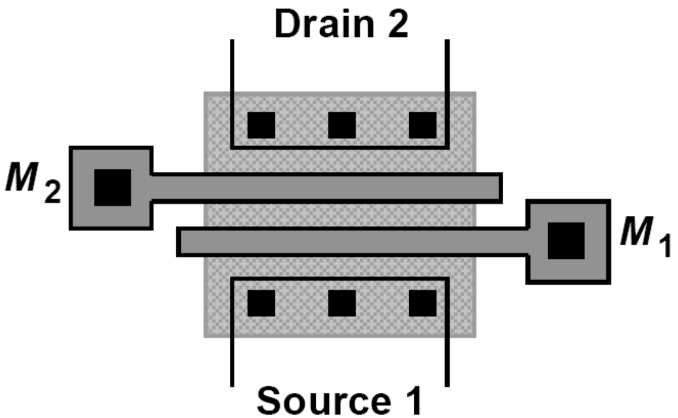
- In the third step, the bias of M_1 is defined by means of M_B and I_{REF}

Design Procedure (III)

➢ **Next, the width of M_2 must be chosen**

The optimum width of M_2 is likely to be near that of M_1

In order to minimize the capacitance at node X, transistors M_1 and M_2 can be laid out such that the drain area of the former is shared with the source area of the latter.



➢ **In the last step, the value of the load inductor, L_1, must be determined**

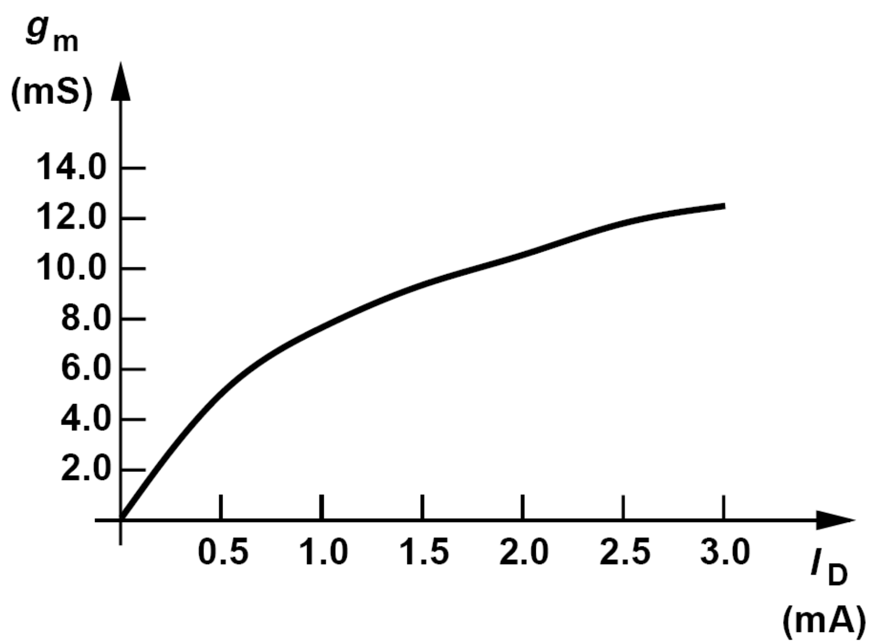
In a manner similar to the choice of L_B, we compute L_1 such that it resonates with C_{GD2} + C_{DB2}, the input capacitance of the next stage, and its own capacitance.

LNA Design Example (Ⅰ)

Design the LNA for a center frequency of 5.5 GHz in 65-nm CMOS technology. Assume the circuit is designed for an 11a receiver.

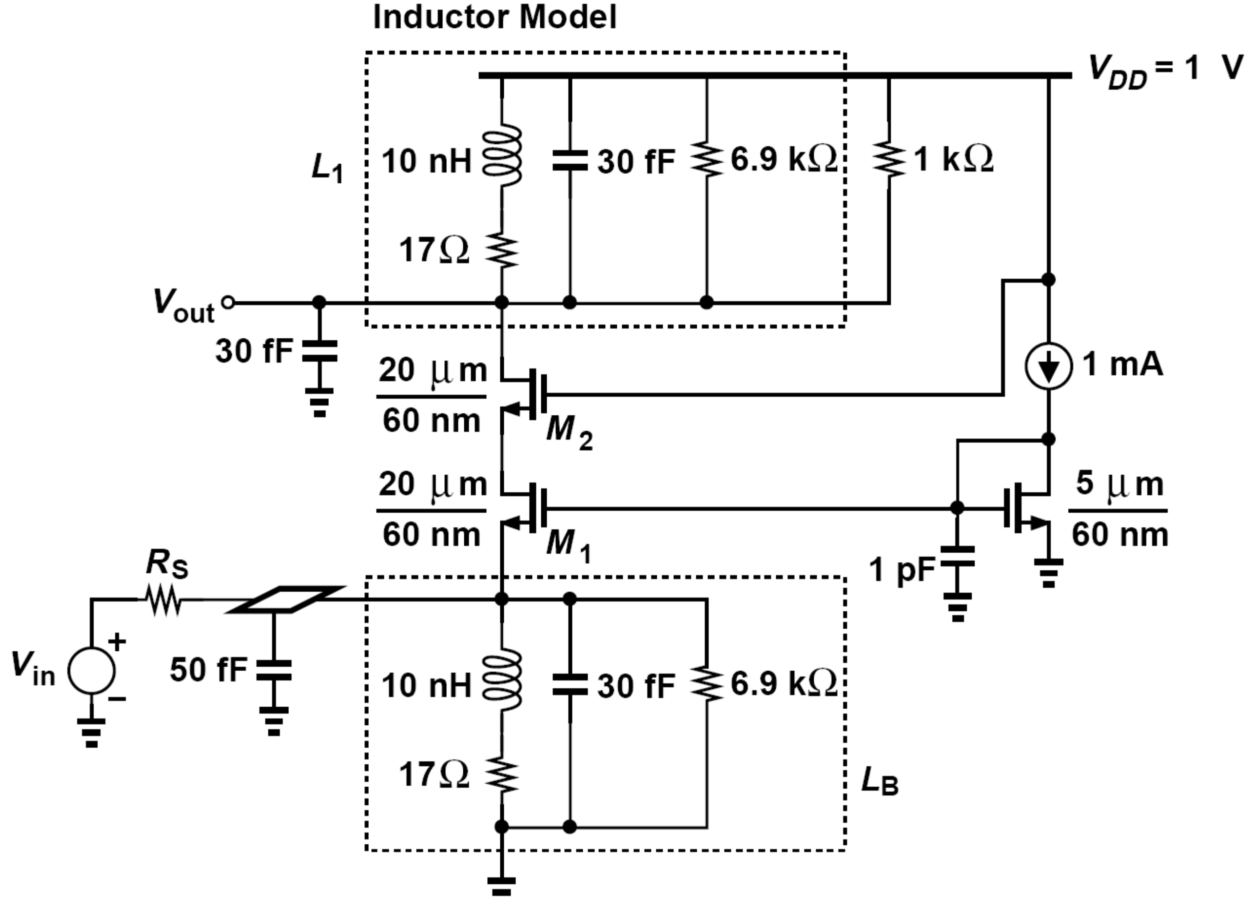
Figure below plots the transconductance of an NMOS transistor with W = 10 μm and L = 60 nm as a function of the drain current. We select a bias current of 2 mA to achieve a g_m of about 10 mS = 1/(100Ω).

Thus, to obtain an input resistance of 50 Ω, we must double the width and drain current. The capacitance introduced by a 20-μm transistor at the input is about 30 fF. To this we add a pad capacitance of 50 fF and choose L_B = 10 nH for resonance at 5.5 GHz.



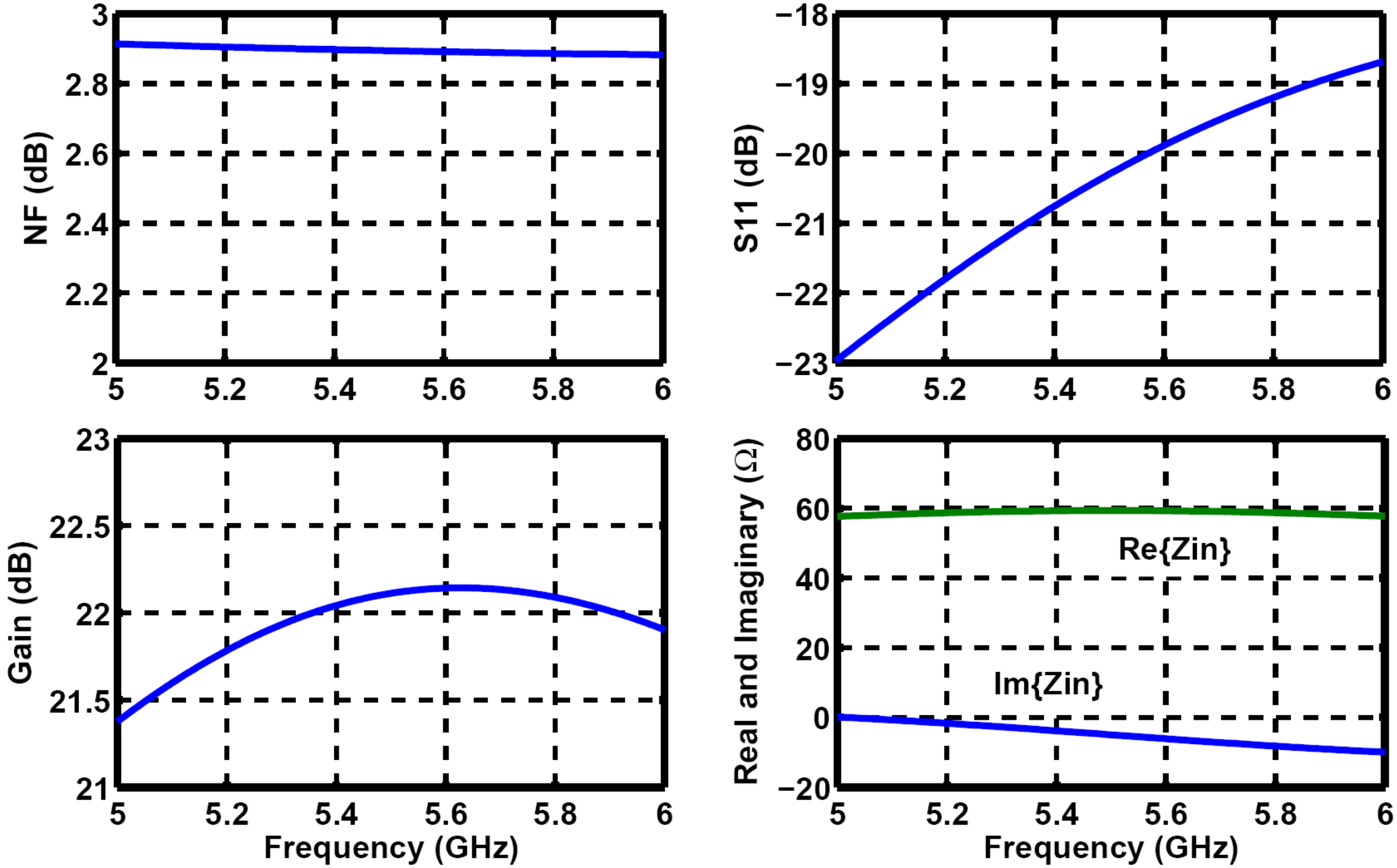
LNA Design Example (Ⅱ)

Next, we choose the width of the cascode device equal to 20 *μ*m and assume a load capacitance of 30 fF. This allows the use of a 10-nH inductor for the load, too, because the total capacitance at the output node amounts to about 75 fF. However, with a *Q* of about 10 for such an inductor, the LNA gain is excessively high and its bandwidth excessively low. For this reason, we place a resistor of 1 kΩ in parallel with the tank. Figure below shows the design details.



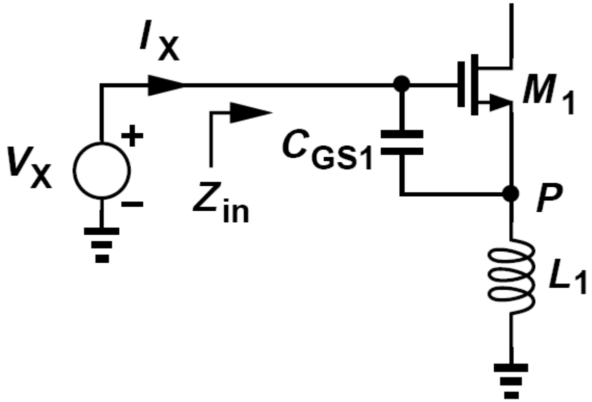
LNA Design Example (III)

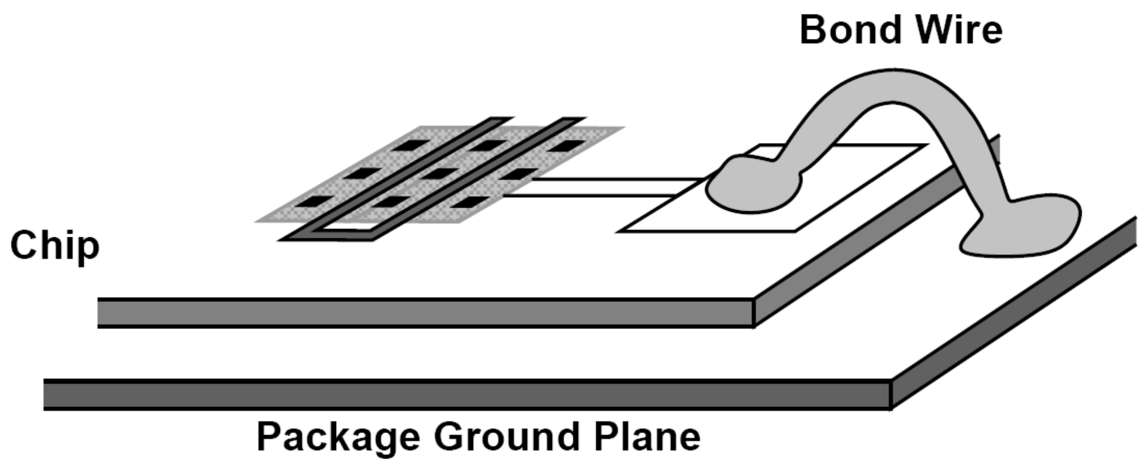
The inductor loss is modeled by series and parallel resistances so as to obtain a broadband representation. The simulation results reveal a relatively flat noise figure and gain from 5 to 6 GHz. The input return loss remains below -18 dB for this range even though we did not refine the choice of L_B.



Cascode CS Stage with Inductive Degeneration: Input Impedance

The feedback through the gate-drain capacitance many be exploited to produce the required real part but it also leads to a negative resistance at lower frequencies.





We have:

$$V_P = \left(I_X + \frac{g_m I_X}{C_{GS1} s}\right) L_1 s$$

Since $V_X = V_{GS1} + V_P$

$$\frac{V_X}{I_X} = \frac{1}{C_{GS1} s} + L_1 s + \frac{g_m L_1}{C_{GS1}}$$

Thus, the third term can be chosen equal to 50Ω.

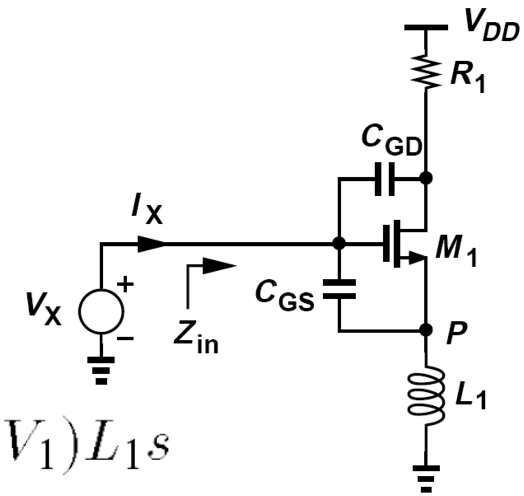
In practice, the degeneration inductor is often realized as a bond wire with the reasoning that the latter is inevitable in packaging and must be incorporated in the design.

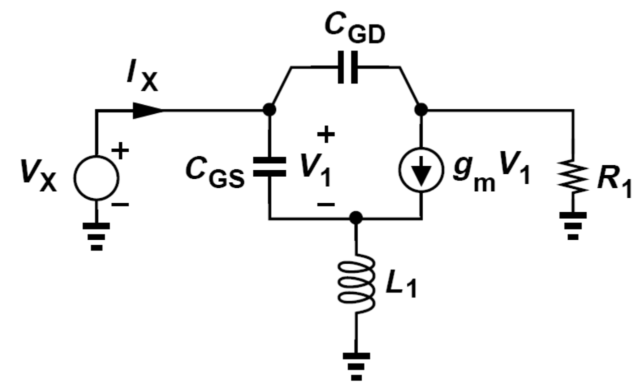
Input Impedance of CS Stage in the Presence of C_{GD}

Determine the input impedance of the circuit shown below (left) if C_{GD} is not neglected and the drain is tied to a load resistance R_1. Assume $R_1 \approx 1/g_m$ (as in a cascode).

Solution:

From equivalent shown here (right):





$$V_X = V_1 + (V_1 C_{GS} s + g_m V_1) L_1 s$$

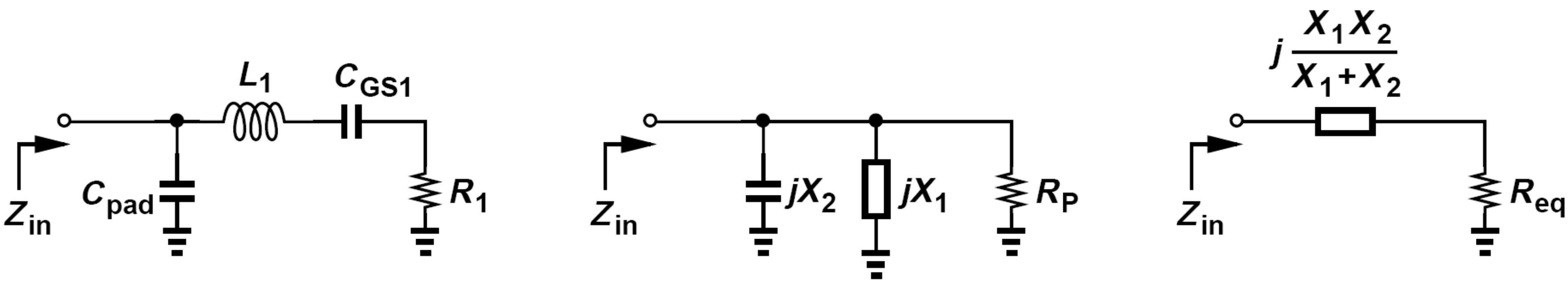
$$V_X = (I_X - V_1 C_{GS} s - g_m V_1) R_1 + (I_X - V_1 C_{GS} s) \frac{1}{C_{GD} s}$$

$$\frac{V_X}{I_X} = \frac{\left(R_1 + \frac{1}{C_{GD} s}\right)(L_1 C_{GS} s^2 + g_m L_1 s + 1)}{L_1 C_{GS} s^2 + (R_1 C_{GS} + g_m L_1) s + g_m R_1 + C_{GS}/C_{GD} + 1}$$

$$\frac{V_X}{I_X} \approx \left(\frac{1}{C_{GS} s} + L_1 s + \frac{g_m L_1}{C_{GS}}\right)\left[1 - \frac{2C_{GD}}{C_{GS}} - L_1 C_{GD} s^2 - \left(R_1 C_{GD} + g_m L_1 \frac{C_{GD}}{C_{GS}}\right) s\right]$$

Effect of Pad Capacitance

- In addition to C_{GD}, the input pad capacitance of the circuit also lowers the input resistance.



$$R_P = \frac{X_1^2}{R_1}$$

We now merge the two parallel reactance and transform the resulting circuit to that shown above (right)

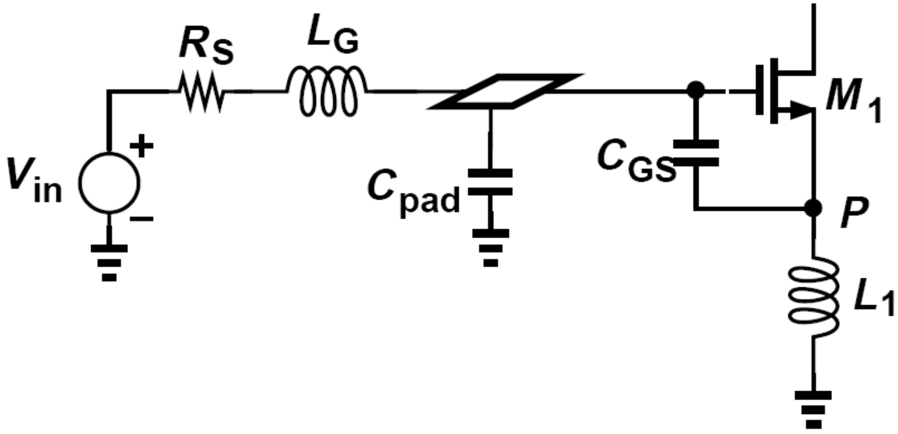
$$\begin{aligned} R_{eq} &= \left(\frac{X_1 X_2}{X_1 + X_2}\right)^2 \cdot \frac{1}{R_P} \\ &= \left(\frac{X_2}{X_1 + X_2}\right)^2 R_1. \end{aligned}$$

$$\Rightarrow R_{eq} \approx \left(\frac{C_{GS1}}{C_{GS1} + C_{pad}}\right)^2 R_1$$

Two Observations on Effect of Pad Capacitance

- **First, the effect of the gate-drain and pad capacitance suggests that the transistor f_T need not be reduced so much as to create R_1 = 50 Ω.**

- **Second, since the degeneration inductance necessary for $Re\{Z_{in}\}$ = 50 Ω is insufficient to resonate with $C_{GS1} + C_{pad}$, another inductor must be placed in series with the gate.**

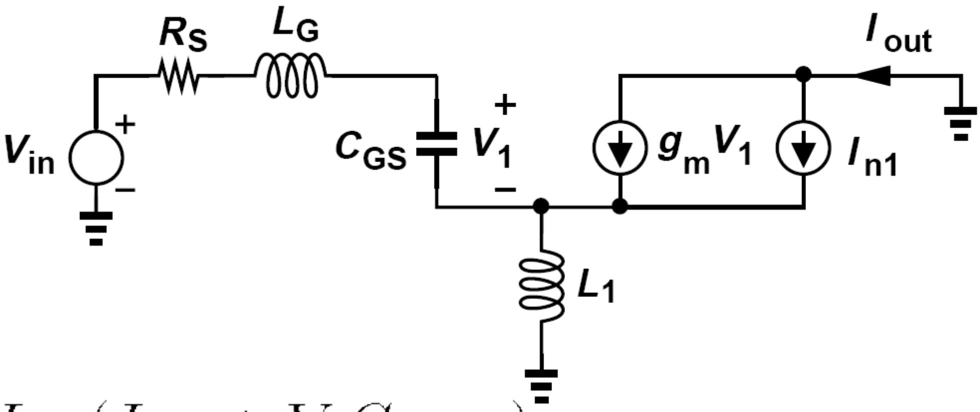


A 5-GHz LNA requires a value of 2 nH for L_G. Discuss what happens if L_G is integrated on the chip and its Q does not exceed 5.

With Q = 5, L_G suffers from a series resistance equal to $L_G\omega/Q$ = 12.6 Ω. This value is not much less than 50 Ω, degrading the noise figure considerably. For this reason, L_G is typically placed off-chip.

NF Calculation (Ⅰ)

Excluding the effect of channel-length modulation, body effect, C_{GD} and C_{pad} for simplicity



$$I_{out} = g_m V_1 + I_{n1}$$

KVL around the input loop yields:

$$V_{in} = (R_S + L_G s)V_1 C_{GS1} s + V_1 + L_1 s(I_{out} + V_1 C_{GS1} s)$$

$$V_{in} = I_{out} L_1 s + \frac{(L_1 + L_G)C_{GS1} s^2 + 1 + R_S C_{GS1} s}{g_m}(I_{out} - I_{n1})$$

$$V_{in} = I_{out}\left(jL_1\omega_0 + \frac{jR_S C_{GS1}\omega_0}{g_m}\right) - I_{n1}\frac{jR_S C_{GS1}\omega_0}{g_m}$$

The coefficient of I_{out} represents the transconductance gain of the circuit:

$$\left|\frac{I_{out}}{V_{in}}\right| = \frac{1}{\omega_0\left(L_1 + \frac{R_S C_{GS1}}{g_m}\right)}$$

NF Calculation (Ⅱ)

$$\left|\frac{I_{out}}{V_{in}}\right| = \frac{\omega_T}{2\omega_0} \cdot \frac{1}{R_S}$$

Interestingly, the transconductance of the circuit remains independent of L_1, L_G, and g_m so long as the input is matched.

$$|I_{n,out}|_{M1} = |I_{n1}| \frac{R_S C_{GS1}}{g_m L_1 + R_S C_{GS1}}$$

For $g_m L_1 / C_{GS1} = R_S$

$$|I_{n,out}|_{M1} = \frac{|I_{n1}|}{2}$$

$$\overline{I^2_{n,out}}|_{M1} = kT\gamma g_m$$

We arrive at the noise figure of the circuit:

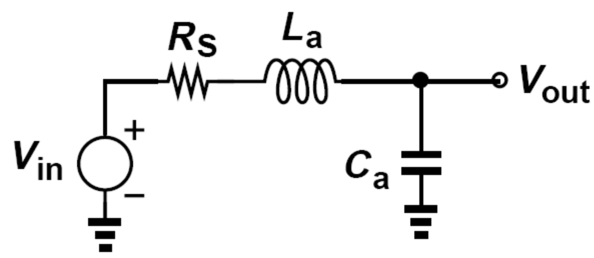
$$\mathrm{NF} = 1 + g_m R_S \gamma \left(\frac{\omega_0}{\omega_T}\right)^2$$

- **It is important to bear in mind that this result holds only at the input resonance frequency and if the input is matched.**

Example of NF and Power Dissipation

A student notes from equation above that, if the transistor width and bias current are scaled down proportionally, then gm and C_{GS1} decrease while $g_m/C_{GS1} = \omega_T$ remains constant. That is, the noise figure decreases while the power dissipation of the circuit also decreases! Does this mean we can obtain NF = 1 with zero power dissipation?

As C_{GS1} decreases, $L_G + L_1$ must increase proportionally to maintain a constant ω_0. Suppose L_1 is fixed and we simply increase L_G. As C_{GS1} approaches zero and L_G infinity, the Q of the input network ($\approx L_G\omega_0/R_S$) also goes to infinity, providing an infinite voltage gain at the input. Thus, the noise of R_S overwhelms that of M_1, leading to NF = 1. This result is not surprising; after all, $|V_{out}/V_{in}| = (R_S C_a \omega_0)^{-1}$ at resonance, implying that the voltage gain approaches infinity if C_a goes to zero (and L_a goes to infinity so that ω_0 is constant). In practice, of course, the inductor suffers from a finite Q (and parasitic capacitances), limiting the performance.



What if we keep L_G constant and increase the degeneration inductance, L_1? The NF still approaches 1 but the transconductance of the circuit, falls to zero if C_{GS1}/g_m remains fixed. That is, the circuit provides a zero-dB noise figure but with zero gain.

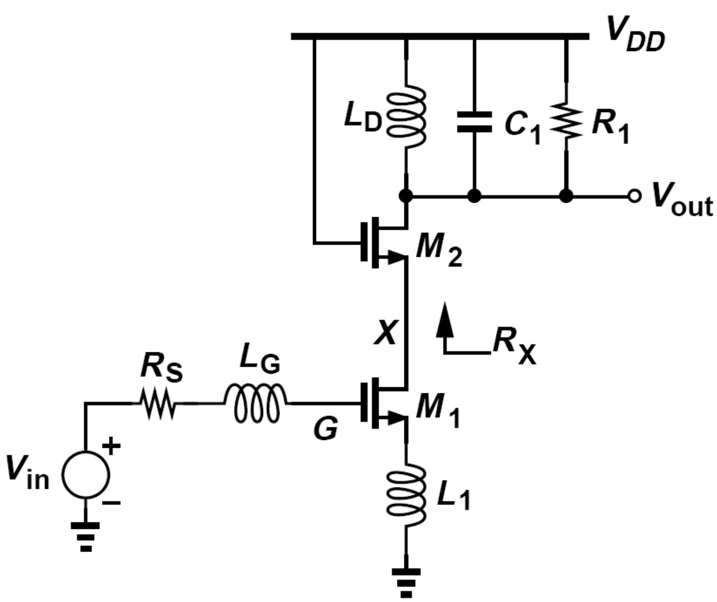
Cascode CS Stage with Inductive Degeneration

Add a cascode transistor in the output branch to suppress the effect of negative resistance.

The voltage gain:

$$\frac{V_{out}}{V_{in}} = \frac{\omega_T}{2\omega_0}\frac{R_1}{R_S}$$

$$= \frac{R_1}{2L_1\omega_0}.$$



The impedance seen at the source of M_2, R_X rises sharply at the output resonance frequency.

$$R_X = \frac{R_1 + r_{O2}}{1 + g_m r_{O2}}$$

The voltage gain from the gate to the drain of *M_1*:

$$\frac{V_X}{V_G} = \frac{R_S}{L_1\omega_0} \cdot \frac{R_1 + r_{O2}}{(1 + g_{m2}r_{O2})(R_S + L_G\omega_0)}$$

Design Procedure (Ⅰ)

- The procedure begins with four knowns: the frequency of operation, ω_0, the value of the degeneration inductance, L_1, the input pad capacitance, C_{pad}, and the value of the input series inductance, L_G.

Governing the design are the following equations:

$$\frac{1}{(L_G + L_1)(C_{GS1} + C_{pad})} = \omega_0^2$$

$$\left(\frac{C_{GS1}}{C_{GS1} + C_{pad}}\right)^2 L_1\omega_T = R_S.$$

- In the next step, the dimensions of the cascode device are chosen equal to those of the input transistor.

- The design procedure continues with selecting a value for L_D such that it resonates at ω_0 with the drain-bulk and drain-gate capacitances of M_2, the input capacitance of the next stage, and the inductors's own parasitic capacitance.

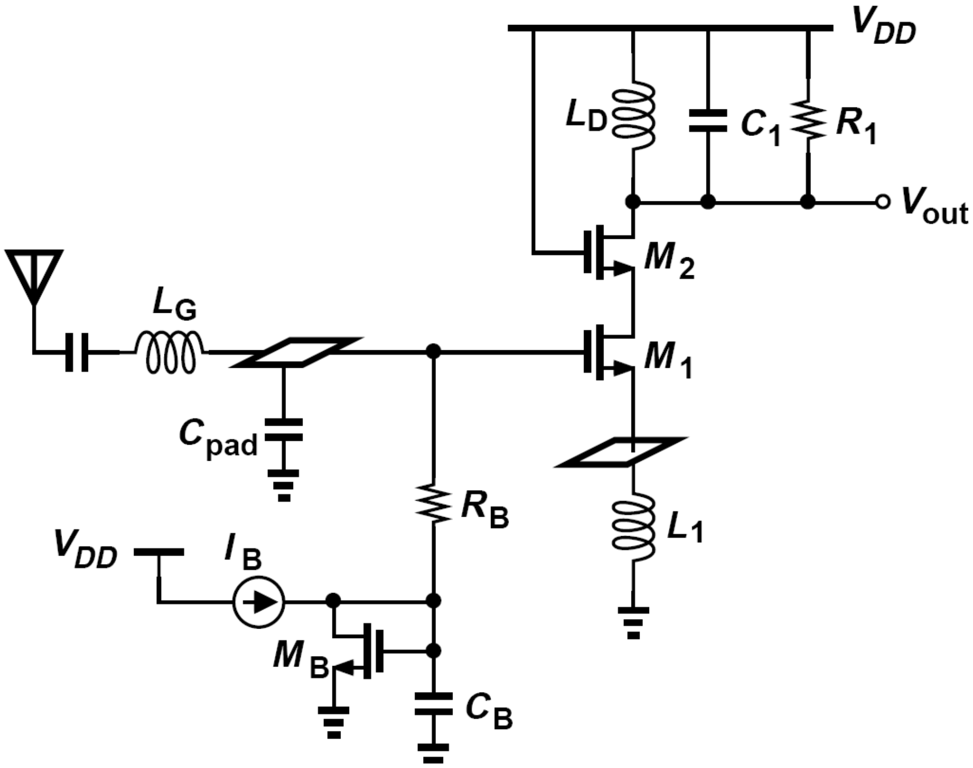
Design Procedure (Ⅱ)

- **In the last step of the design, we must examine the input match. Due to the Miller multiplication of C_{GD1}, it is possible that the real and imaginary parts depart from their ideal values, necessitating some adjustment in L_G.**

Alternatively, the design procedure can begin with known values for NF and L_1 and the following two equations:

$$
\begin{aligned}
NF &= 1 + g_{m1} R_S \gamma \left(\frac{\omega_0}{\omega_T}\right)^2 \\
R_S &= \left(\frac{C_{GS1}}{C_{GS1} + C_{pad}}\right)^2 L_1 \omega_T;
\end{aligned}
$$

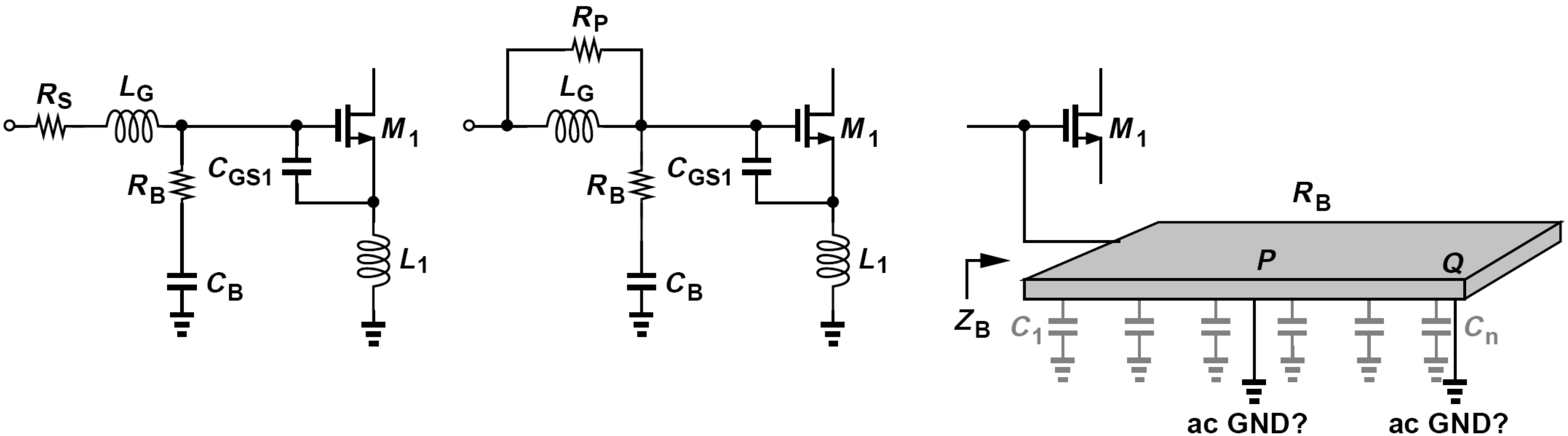
The overall LNA appears as shown on right:



Example of Choosing R_B

How is the value of R_B chosen in figure above?

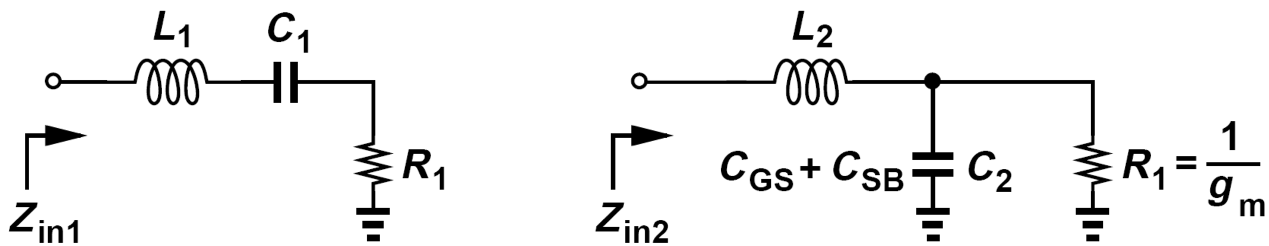
Since R_B appears in parallel with the signal path, its value must be maximized. Is R_B = 10R_S sufficiently high? As illustrated in figure below, the series combination of R_S and L_G can be transformed to a parallel combination with $R_P \approx Q^2R_S \approx (L_G\omega_0/R_S)^2R_S$. We note that a voltage gain of, say, 2 at the input requires Q = 3, yielding $R_P \approx$ 450 Ω. Thus, R_B = 10R_S becomes comparable with R_P , raising the noise figure and lowering the voltage gain. R_B must remain much greater than R_P .



Large resistors may suffer from significant parasitic capacitance. However, increasing the length of a resistor does not load the signal path anymore even though it leads to a larger overall parasitic capacitance.

Comparison Between Input Matching Bandwidth for CG and CS Stage

It is believed that input matching holds across a wider bandwidth for the CG stage than for the inductively degenerated CS stage. Is this statement correct?



For the CS stage (left)

$$Re\{Z_{in1}\} = R_1$$

$$Im\{Z_{in1}\} = \frac{L_1 C_1 \omega^2 - 1}{C_1 \omega}$$

If the center frequency of interest is ω_0

$$Im\{Z_{in1}\} \approx 2 L_1 \Delta\omega \frac{L_1 \Delta\omega}{\omega_0}$$

For the CG stage (right), on the other hand:

$$Re\{Z_{in2}\} = \frac{R_1}{1 + R_1^2 C_2^2 \omega^2}$$

$$Im\{Z_{in2}\} = L_2 \omega - \frac{R_1^2 C_2 \omega}{1 + R_1^2 C_2^2 \omega^2}$$

For $\omega << \omega_T$

$$Re\{Z_{in2}\} \approx R_1$$

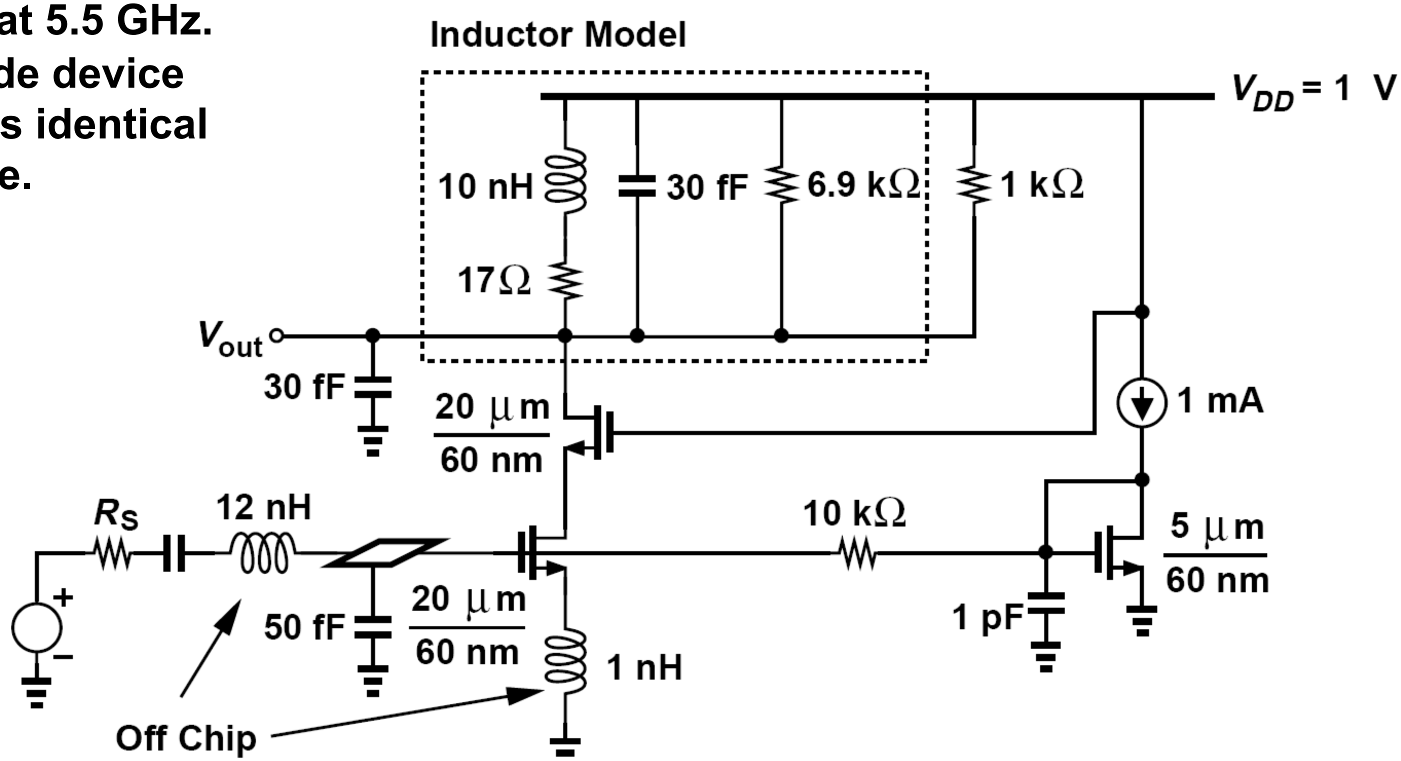
$$Im\{Z_{in2}\} \approx (L_2 - R_1^2 C_2)\omega$$

Design Example of Cascode CS LNA (Ⅰ)

Design a cascode CS LNA for a center frequency of 5.5 GHz in 65-nm CMOS technology.

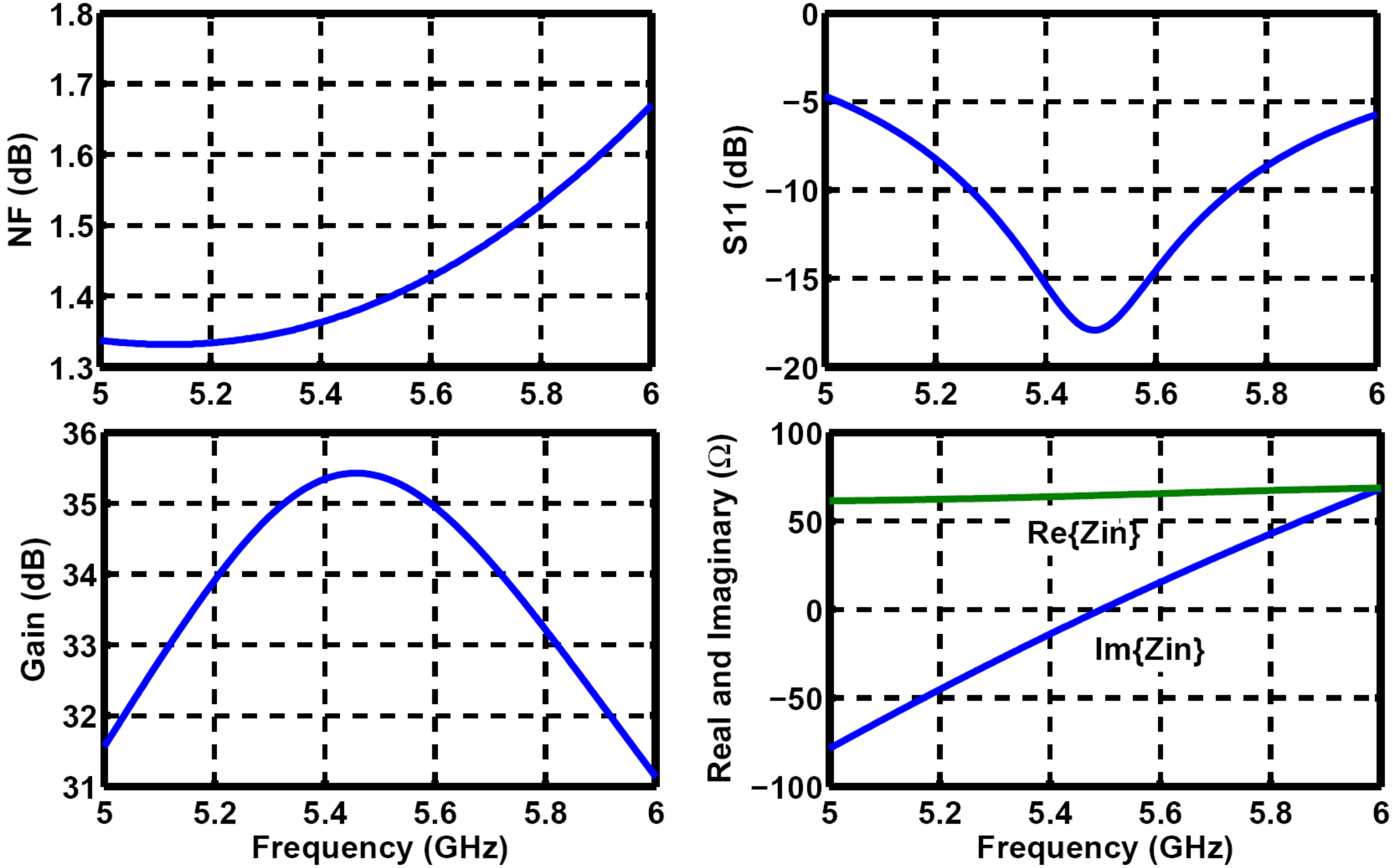
We begin with a degeneration inductance of 1 nH and the same input transistor as that in the CG stage in previous example. Interestingly, with a pad capacitance of 50 fF, the input resistance happens to be around 60Ω. (Without the pad capacitance, $Re\{Z_{in}\}$ is in the vicinity of 600 Ω.) We thus simply add enough inductance in series with the gate (L_G = 12 nH) to null the reactive component at 5.5 GHz.

The design of the cascode device and the output network is identical to that of the CG example.



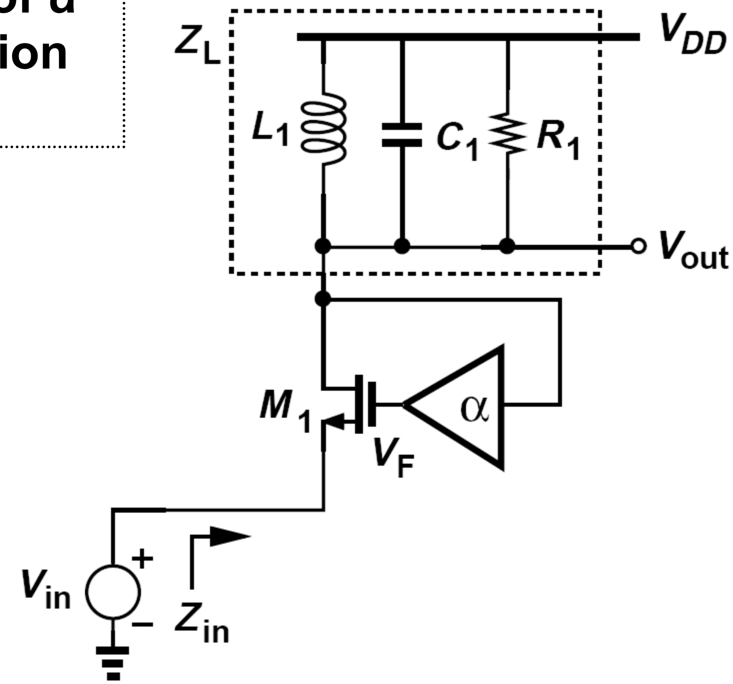
Design Example of Cascode CS LNA (Ⅱ)

Figure below shows the simulated characteristics. We observe that the CS stage has a higher gain, a lower noise figure, and a narrower bandwidth than the CG stage in previous example.



Variants of Common-Gate LNA: CG LNA with Feedback (Ⅰ)

- The block having a gain (or attenuation factor) of *α* senses the output voltage and subtracts a fraction thereof from the input.

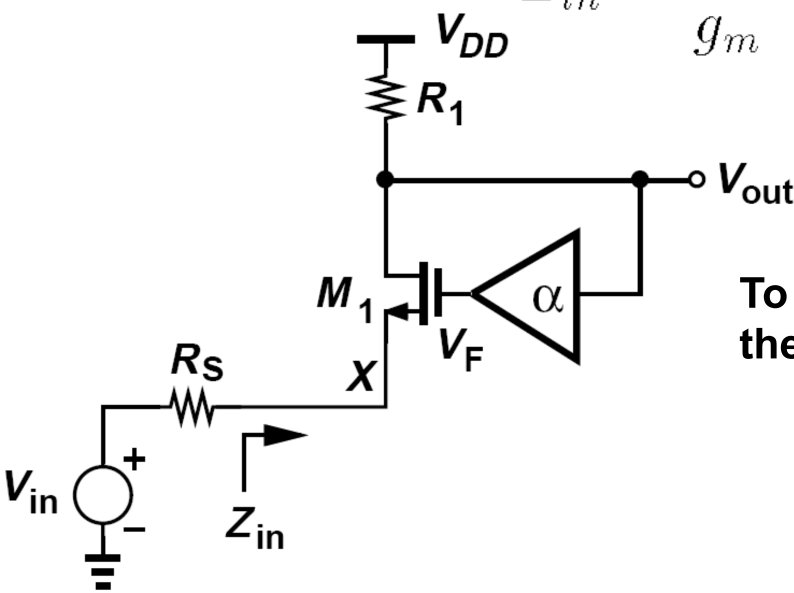


If channel length modulation and body effect are neglected, the closed-loop input impedance is equal to:

$$Z_{in} = \frac{1}{g_m} + \alpha Z_L$$

At resonance,

$$Z_{in} = \frac{1}{g_m} + \alpha R_1$$

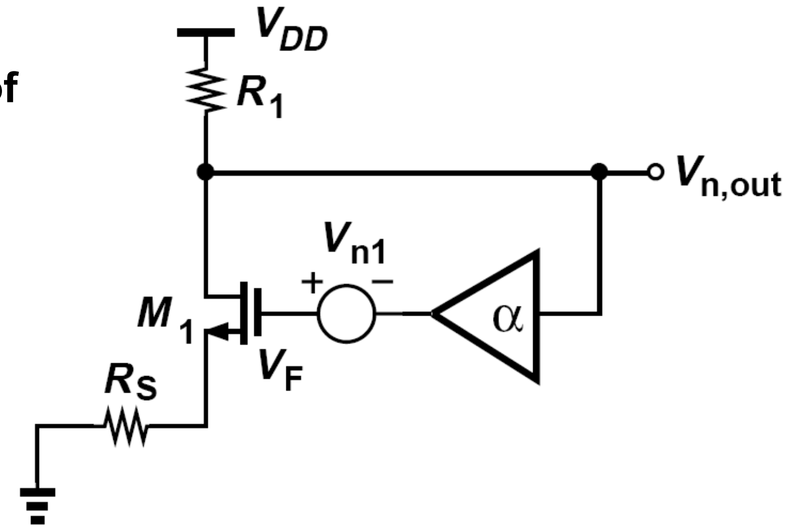


To calculate noise figure, we first calculate the gain with the aid of the circuit on the left.

$$V_{n,out}|_{M1} = \frac{-g_m V_{n1}}{g_m(\alpha + \frac{R_S}{R_1}) + \frac{1}{R_1}}$$

Variants of Common-Gate LNA: CG LNA with Feedback (Ⅱ)

For output noise calculation, we construct the circuit of figure on the right



$$g_m\left(\alpha V_{n,out} + V_{n1} + \frac{R_S}{R_1}V_{n,out}\right) = -\frac{V_{n,out}}{R_1}$$

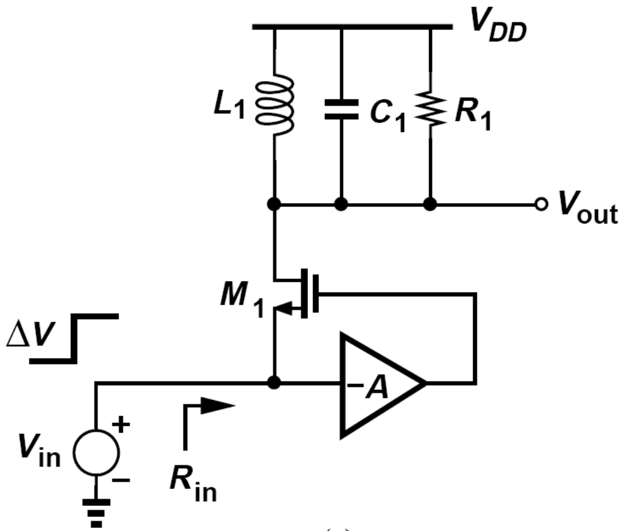
$$\frac{V_{out}}{V_{in}} = \frac{Z_{in}}{Z_{in}+R_S}\cdot\frac{g_m R_1}{1+\alpha g_m R_1}$$

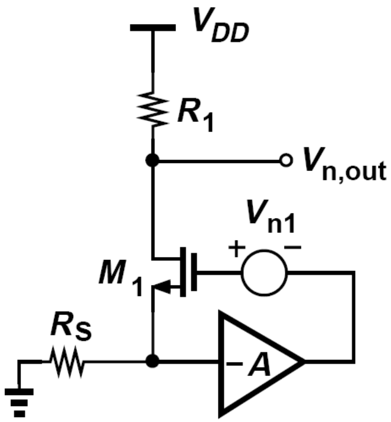
$$= \frac{R_1}{\dfrac{1}{g_m}+\alpha R_1 + R_S},$$

$$\text{NF} = 1 + \frac{\gamma}{g_m R_S} + \frac{R_S}{R_1}\left(1+\frac{1}{g_m R_S}\right)^2$$

The NF can be lowered by raising g_m

CG LNA with Feedforward





- The block having a gain (or attenuation factor) of *α* senses the output voltage and subtracts a fraction thereof from the input.

$$g_m\left(A\frac{R_S}{R_1}V_{n,out}+V_{n1}+\frac{R_S}{R_1}V_{n,out}\right)=-\frac{V_{n,out}}{R_1}$$

$$V_{n,out}|_{M1}=\frac{-g_mR_1V_{n1}}{(1+A)g_mR_S+1}$$

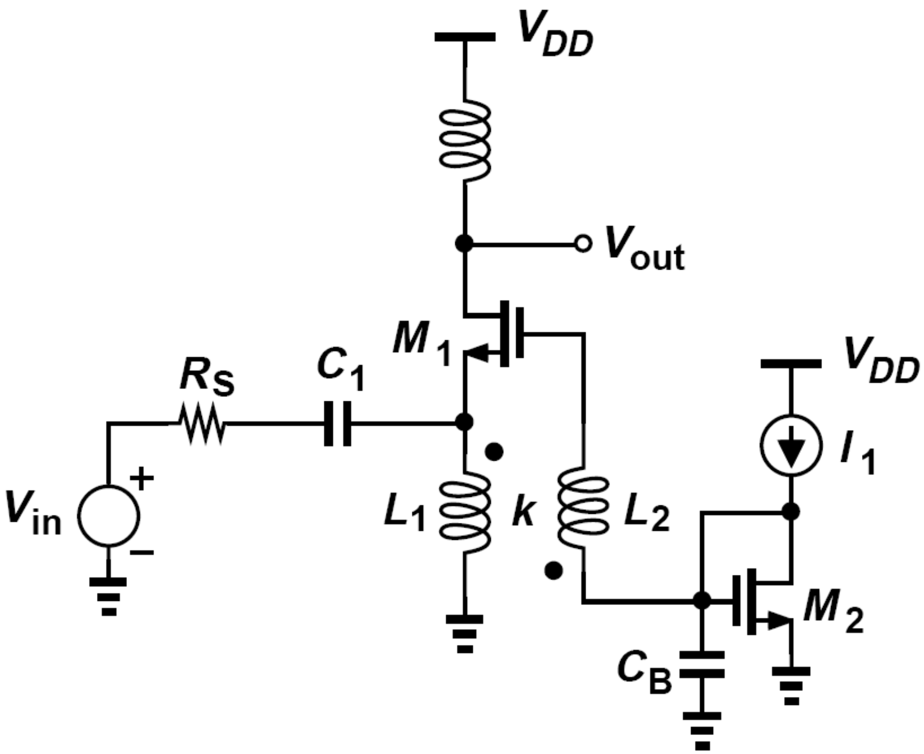
$$\text{NF}=1+\frac{\gamma}{1+A}+\frac{4R_S}{R_1}$$

with the noise of the gain stage A:

$$\text{NF}=1+\frac{\gamma}{1+A}+\frac{4R_S}{R_1}+\frac{A^2}{(1+A)^2}\frac{\overline{V_{nA}^2}}{4kTR_S}$$

CG Stage with Transformer Feedforward

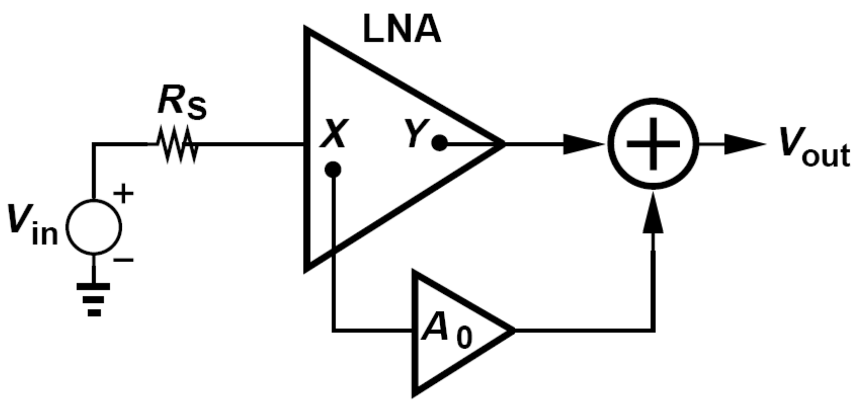
- For a coupling factor of *k* between the primary and the secondary and a turns ratio of *n*, the transformer provides a voltage gain of *kn*.



- On-chip transformer geometries make it difficult to achieve a voltage gain higher than roughly 3, even with stacked spirals

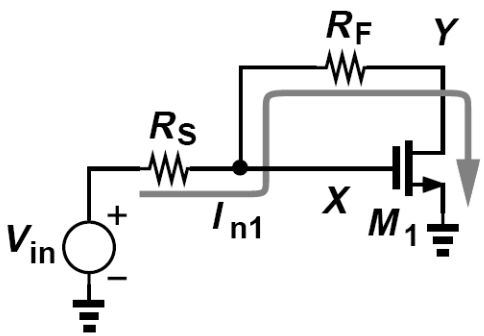
Noise-Canceling LNAs: Basic Ideas

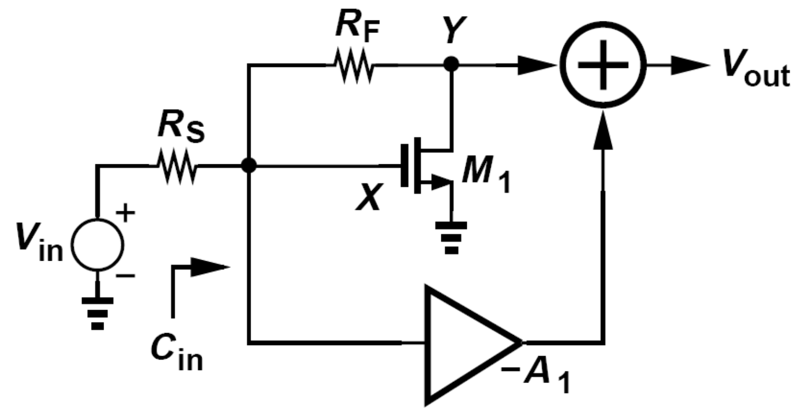
- "Noise-canceling LNAs" aim to cancel the term representing the contribution of the input transistor in the noise figure of LNAs.



- First identify two nodes at which the signal appears with opposite polarities but the noise of the input transistor appears with the same polarity.
- Then their voltages can be properly scaled and summed such that the signal components add and the noise components cancel.

Noise-Canceling LNAs: Noise Figure





The NF can be lowered by raising g_m

$$\frac{V_{out}}{V_X} = 1 - \frac{R_F}{R_S} - \left(1 + \frac{R_F}{R_S}\right) = -\frac{2R_F}{R_S},$$

We obtain the noise figure as:

$$NF = 1 + \frac{R_S}{R_F} + A_1^2\overline{V_{nA1}^2}\frac{R_S}{4kTR_F^2}$$

Since $A_1 = 1 + R_F/R_S$

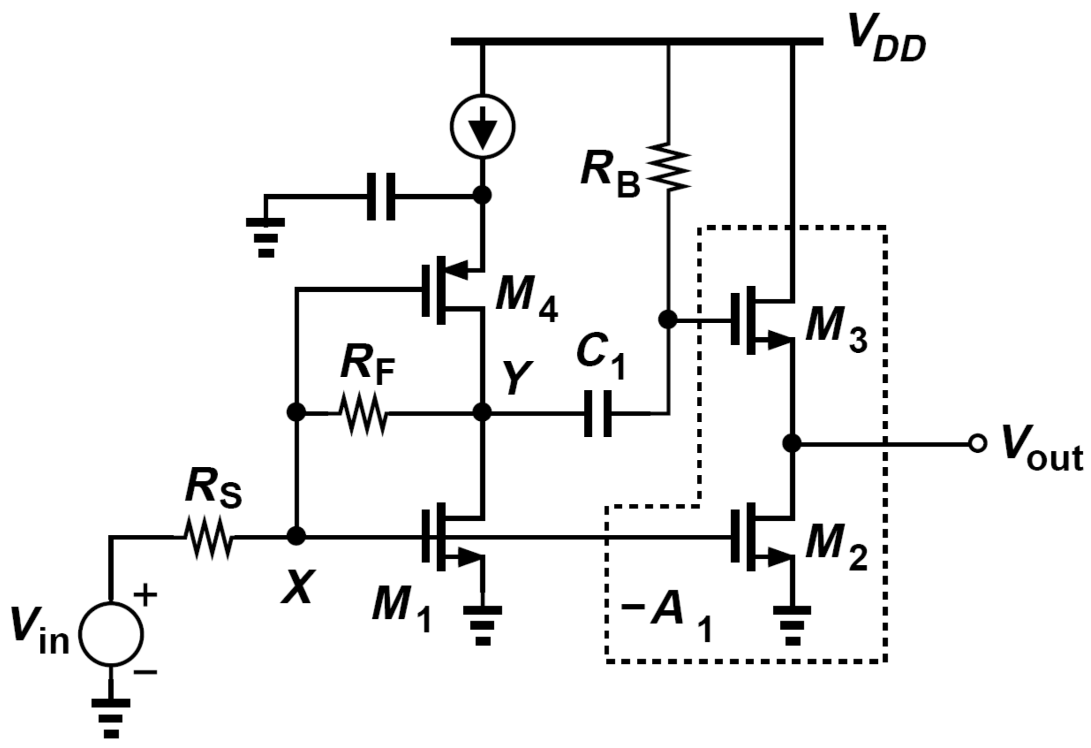
$$NF = 1 + \frac{R_S}{R_F} + \frac{\overline{V_{nA1}^2}}{4kTR_S}\left(1 + \frac{R_S}{R_F}\right)^2$$

Noise-Canceling LNAs: Frequency-Dependent NF and Circuit Implementation

It can be proved that the frequency-dependent noise figure is expressed as

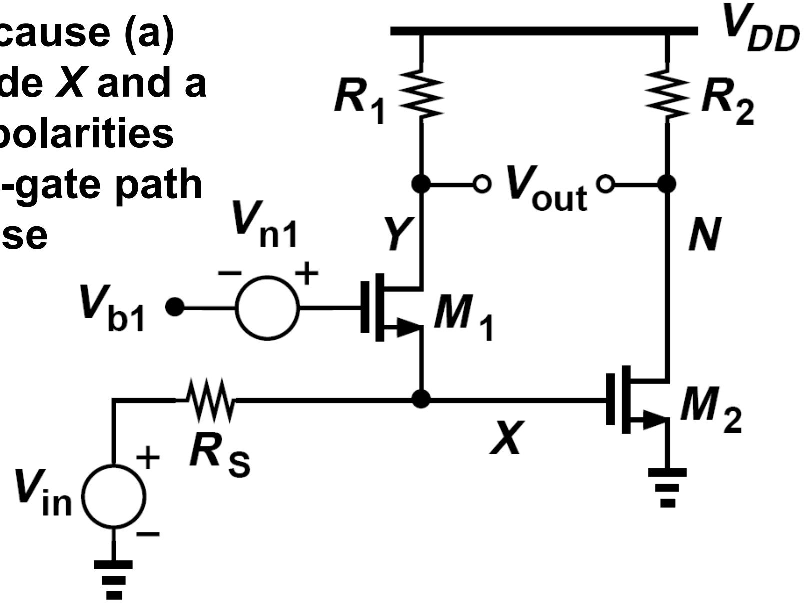
$$\mathrm{NF}(f) = \mathrm{NF}(0) + [\mathrm{NF}(0) - 1 + \gamma]\left(\frac{f}{f_0}\right)^2$$

where NF(0) is given by equation in previous NF calculation and $f_0 = 1/(\pi R_S C_{in})$



Example of an Alternative Implementation

Figure below shows an alternative implementation of a noise-canceling LNA that also performs single ended to differential conversion. Neglecting channel-length modulation, determine the condition for noise cancellation and derive the noise figure.



The circuit follows the noise cancellation principle because (a) the noise of *M_1*, *V_{n1}*, sees a source follower path to node *X* and a common-source path to node *Y*, exhibiting opposite polarities at these two nodes, and (b) the signal sees a common-gate path through *X* and *Y*, exhibiting the same polarity. For noise cancellation, we must have

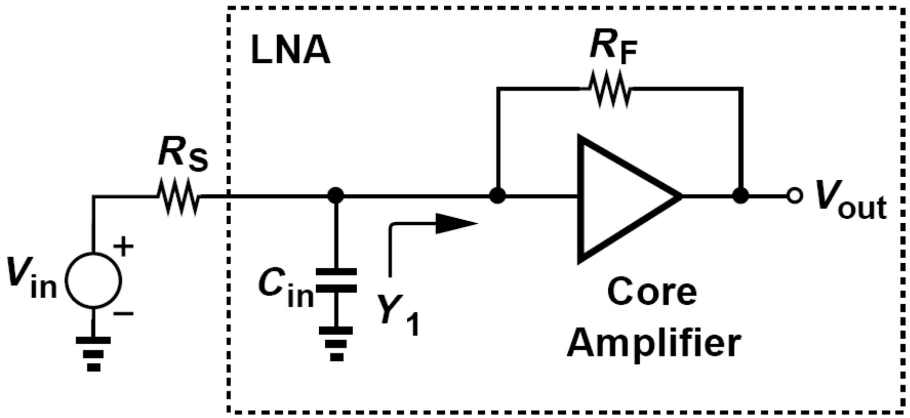
$$g_{m1} R_1 \frac{V_{n1}}{2} = g_{m2} R_2 \frac{V_{n1}}{2}$$

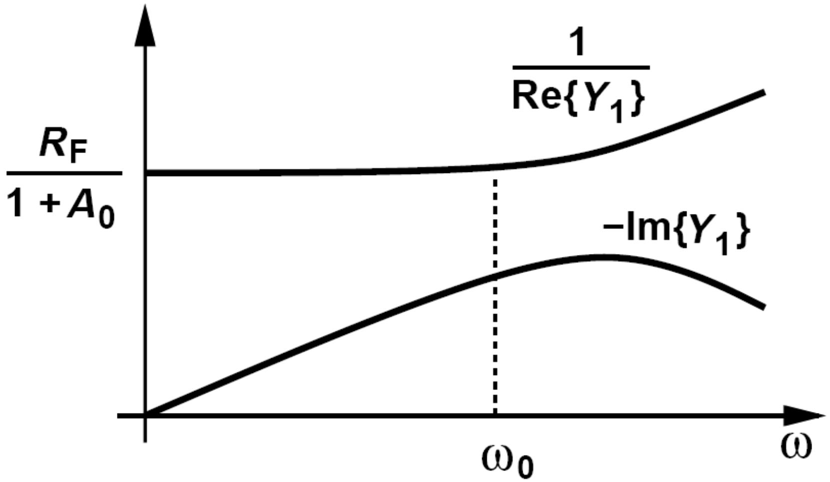
and, since $g_{m1} = 1/R_S$ $\quad R_1 = g_{m2} R_2 R_S$

$$\begin{aligned} \text{NF} &= 1 + \left(\frac{R_S}{R_1}\right)^2 (4kTR_1 + 4kT\gamma g_{m2} R_2^2 + 4kTR_2) \frac{1}{4kTR_S} \\ &= 1 + \frac{R_S}{R_1} + \gamma \frac{R_2}{R_1} + \frac{R_S R_2}{R_1^2}. \end{aligned}$$

Reactance-Cancelling LNAs

- The idea is to exploit the inductive input impedance of a negative-feedback amplifier so as to cancel the input capacitance, C_{in}.





the input admittance is given by

$$Y_1(s) = \frac{s + (A_0 + 1)\omega_0}{R_F(s + \omega_0)}$$

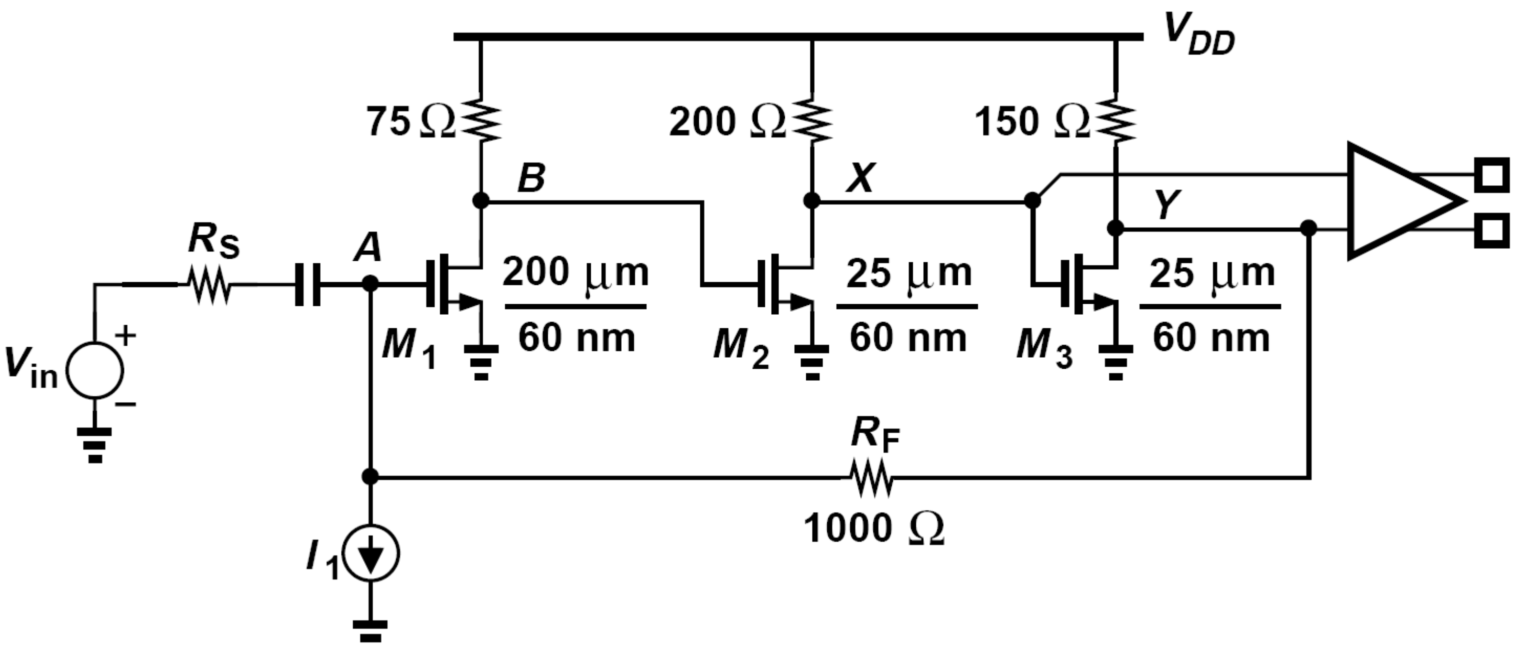
$$\frac{1}{Re\{Y_1\}} = \frac{R_F(\omega^2 + \omega_0^2)}{(1 + A_0)\omega_0^2}$$

$$Im\{Y_1\} = \frac{-A_0\omega\omega_0}{R_F(\omega^2 + \omega_0^2)}$$

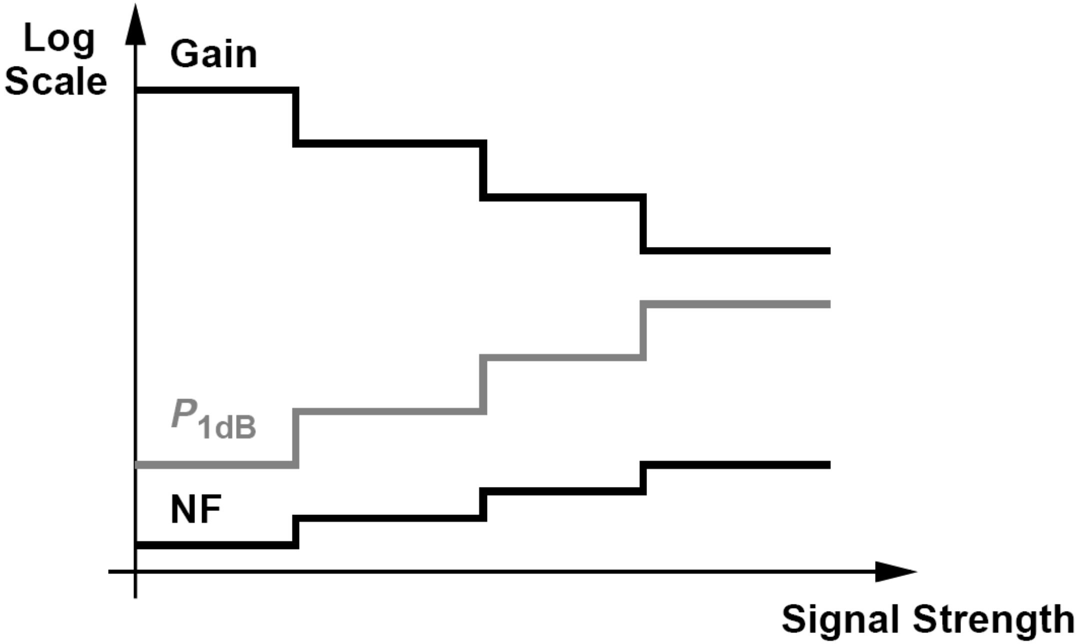
At frequencies well below ω_0, $1/Re\{Y_1\}$ reduces to $R_F/(1+A_0)$, which can be set equal to R_S, and $Im\{Y_1\}$ is roughly $-A_0\omega/(R_F\,\omega_0)$, which can be chosen to cancel $C_{in}\omega$.

Implementation of Reactance-Cancelling LNA

➢ **Three common-source stages provide gain and allow negative feedback. Cascodes and source followers are avoided to save voltage headroom.**



Gain Switching: Effect on NF and P_{1dB}



- Gain switching in an LNA must deal with several issues:

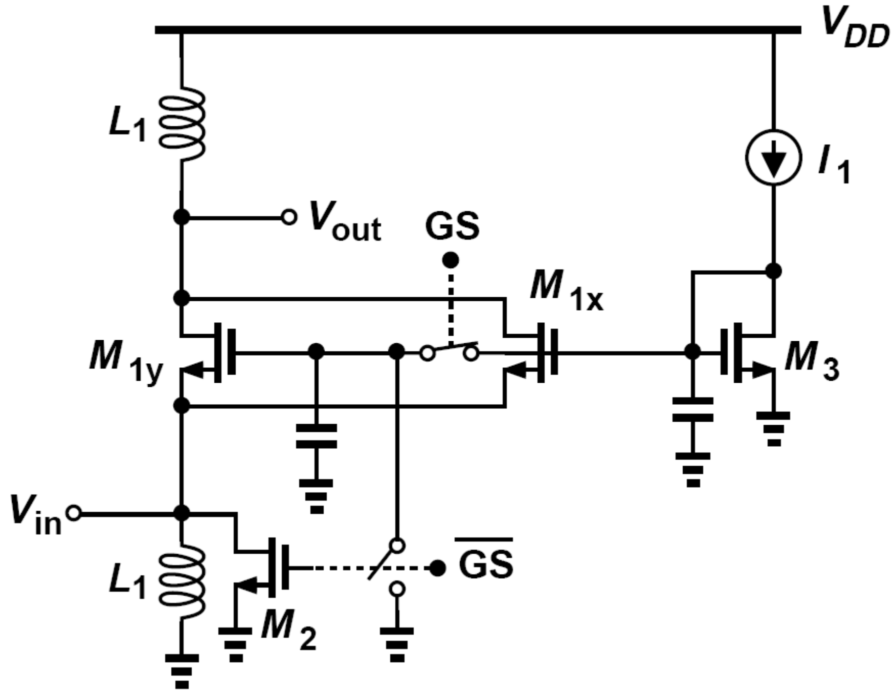
  (1) it must negligibly affect the input matching;

  (2) it must provide sufficiently small "gain steps;"

  (3) the additional devices performing the gain switching must not degrade the speed of the original LNA;

  (4) for high input signal levels, gain switching must make the LNA more linear.

Gain Switching in CG Stage



Choose the devices in the above circuit for a gain step of 3 dB.

Solution:

we have

$$\frac{W_{1x}}{W_{1x}+W_{1y}} = \frac{1}{\sqrt{2}}$$

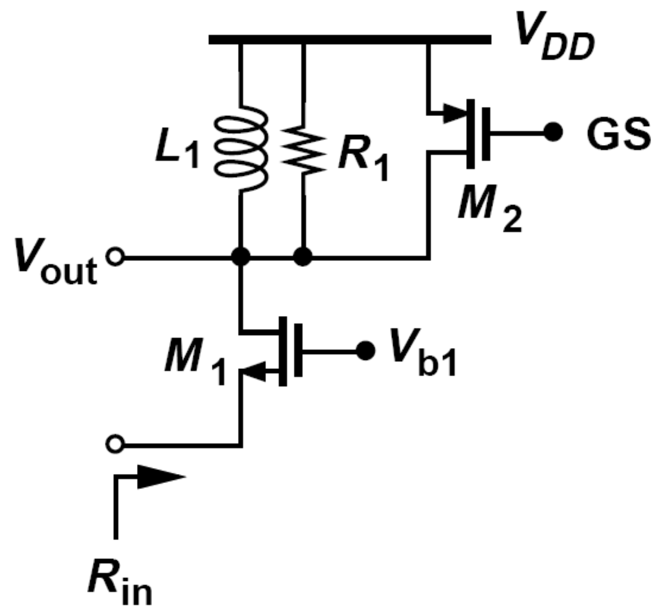
also

$$R_{on2} = \frac{\sqrt{2}}{\sqrt{2}-1} R_S$$

Another Approach to Switching the Gain of a CG Stage

With input matching and in the absence of channel-length modulation, the gain is given by

$$\frac{V_{out}}{V_{in}} = \frac{R_1||R_{on2}}{2R_S}$$



For multiple gain steps, a number of PMOS switches can be placed in parallel with R_1.

Example of the Load Switching Network Design

Design the load switching network of figure above for two 3-dB gain steps.

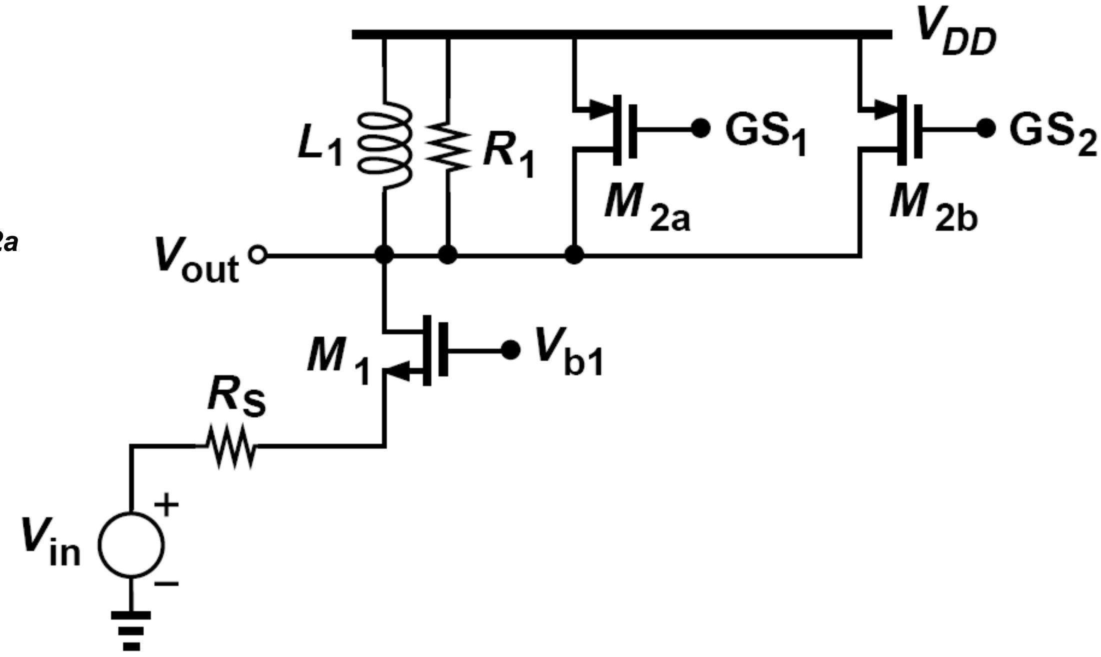
Solution:

As shown in figure below, M_{2a} and M_{2b} switch the gain. For the first 3-dB reduction in gain, M_{2a} is turned on and

$$R_1 || R_{on,a} = \frac{R_1}{\sqrt{2}}$$

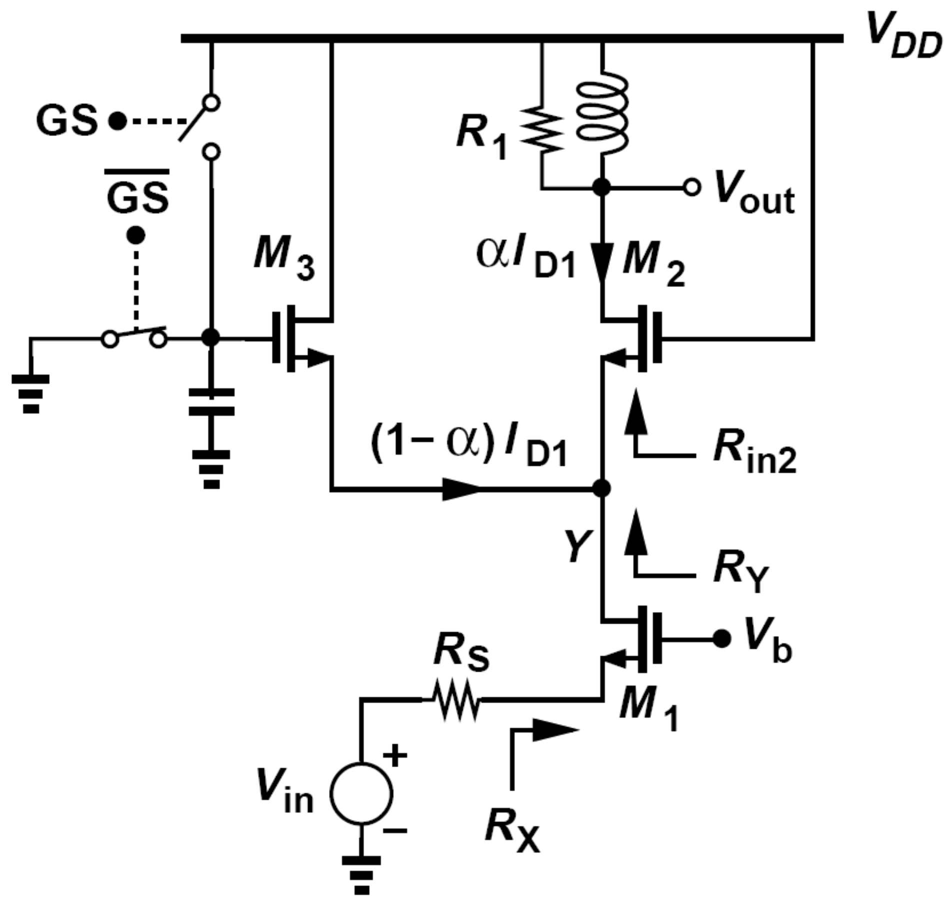
For the second 3-dB reduction, both M_{2a} and M_{2b} are turned on and

$$R_1 || R_{on,a} || R_{on,b} = \frac{R_1}{2}$$



Gain Switching by Cascode Device

- The difficulty that switching the load resistance in a CG stage alters the input resistance can be minimized by adding a cascode transistor.



- The advantage of the above technique over the previous two is that the gain step depends only on W_3/W_2 and not the absolute value of the on-resistance of a MOS switch.
- However, the capacitance introduced by M_3 at node Y degrades the performance at high frequencies.

Example of Input Impedance Changing with Gain

If $W_3 = W_2$ in figure above, how does the input impedance of the circuit change from the high-gain mode to the low-gain mode? Neglect body effect.

Solution:

In the low-gain mode, the impedance seen looking into the source of M_2 changes because both g_{m2} and r_{O2} change. For a square-law device, a twofold reduction in the bias current (while the dimensions remain unchanged) translates to a twofold increase in r_O and a $\sqrt{2}$ reduction in g_m. Thus,

$$R_{in2} = \frac{R_1 + 2r_{O2}}{1 + \sqrt{2}g_{m2}r_{O2}}$$

Where g_{m2} and r_{O2} correspond to the values while M_3 is off. Transistor M_3 presents an impedance of $(1/g_{m3})||r_{O3}$ at Y, yielding

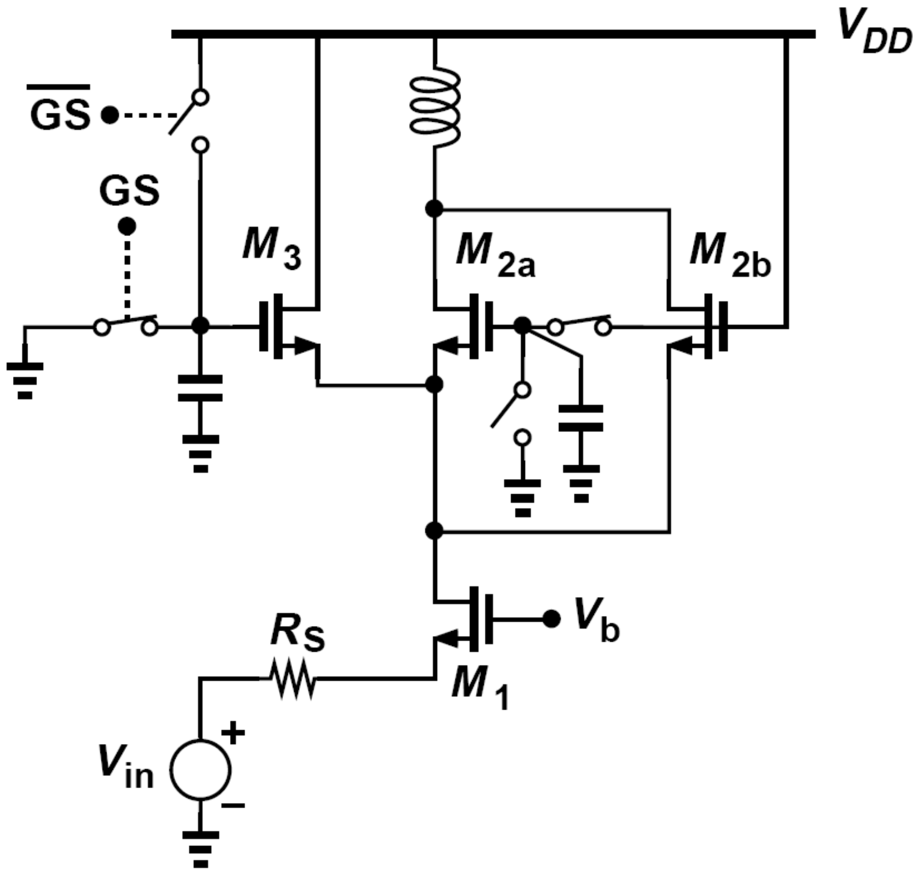
$$R_Y = \frac{1}{g_{m3}}||r_{O3}||\frac{R_1 + 2r_{O2}}{1 + \sqrt{2}g_{m2}r_{O2}}$$

Transistor M_1 transforms this impedance to:

$$R_X = \frac{R_Y + r_{O1}}{1 + g_{m1}r_{O1}}$$

Gain Switching by Programmable Cascode Device

- In order to reduce the capacitance contributed by the gain switching transistor, we can turn off part of the main cascode transistor so as to create a greater imbalance between the two.



Example of Gain Switching Network Design

Design the gain switching network of figure above for two 3-dB steps. Assume equal lengths for the cascode devices.

Solution:

To reduce the gain by 3 dB, we turn on M_3 while M_{2a} and M_{2b} remain on. Thus,

$$1 + \frac{W_3}{W_{2a} + W_{2b}} = \sqrt{2}.$$

For another 3-dB reduction, we turn off M_{2b}:

$$1 + \frac{W_3}{W_{2a}} = 2$$

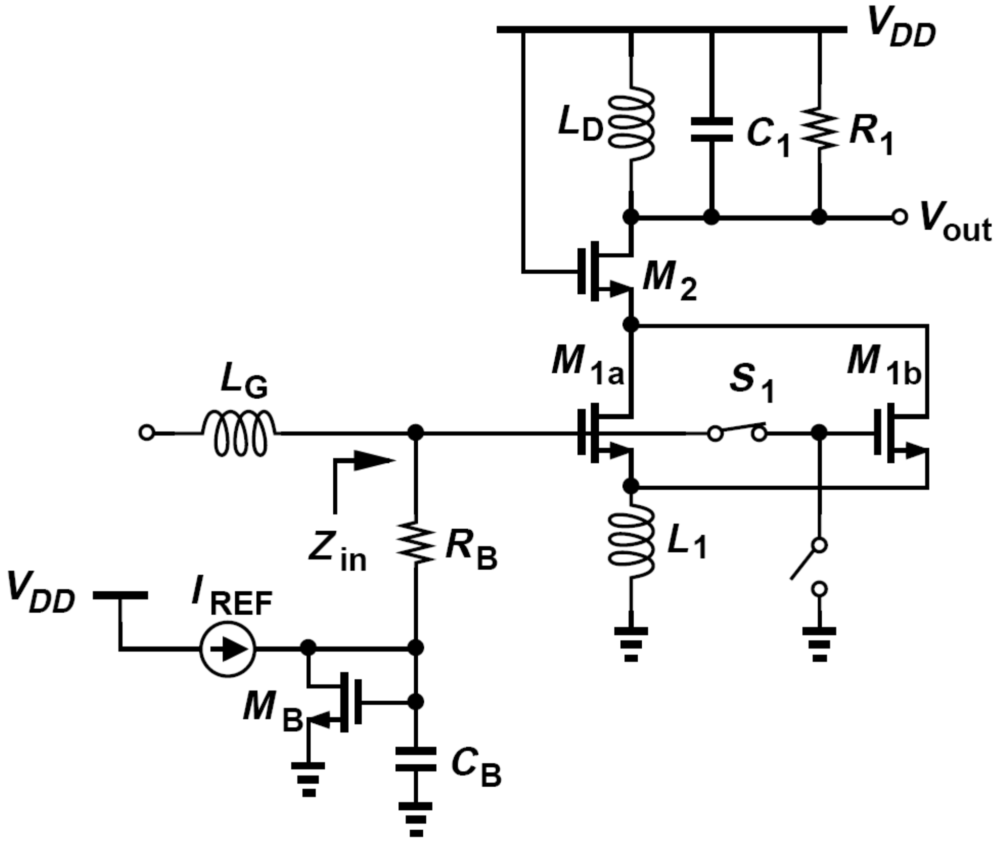
It follows

$$W_3 = W_{2a} = \frac{W_{2b}}{\sqrt{2}}$$

In a more aggressive design, M_2 would be decomposed into three devices, such that one is turned off for the first 3-dB step, allowing M_3 to be narrower.

Gain Switching in Inductively-Degenerated Cascode LNA

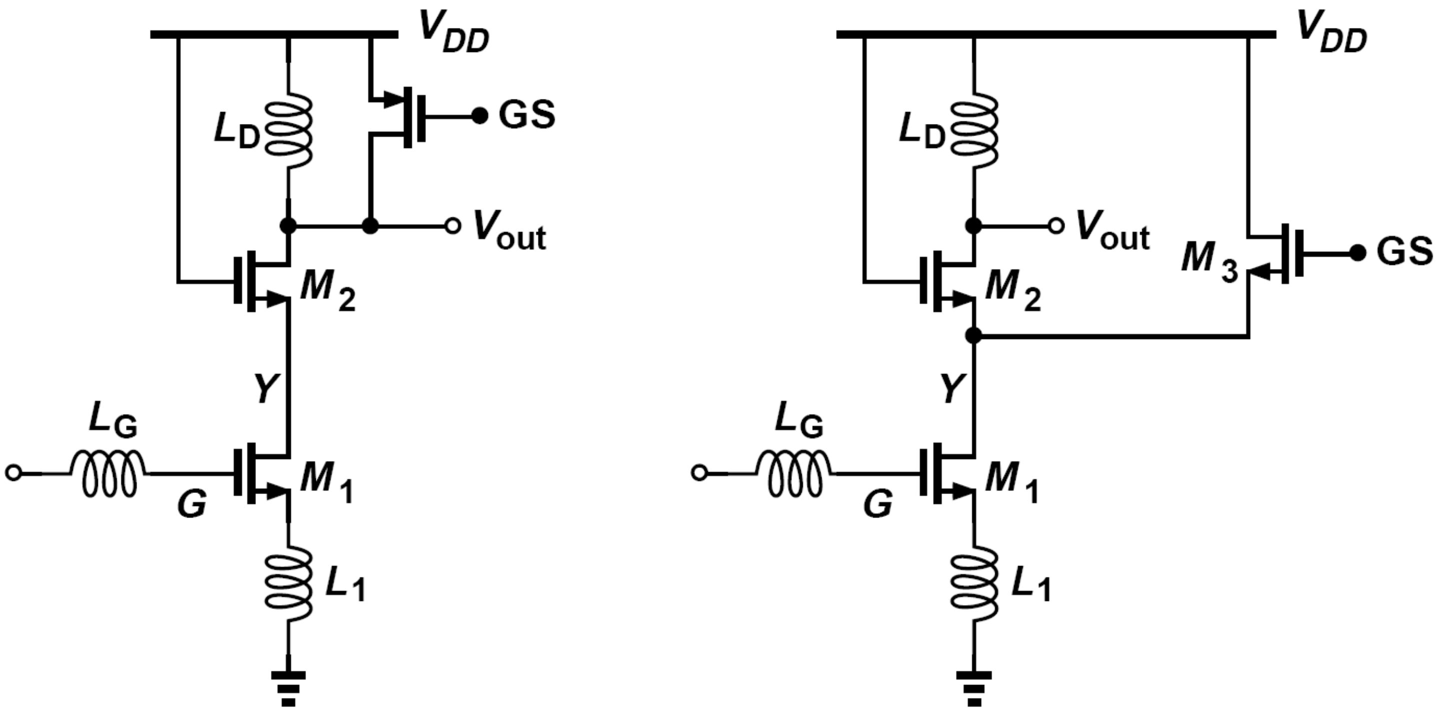
Can we switch part of the input transistor to switch the gain?



- **Turning M_{1b} off degrades the input match. If the input match is somehow restored, then the voltage gain does not change.**
- **Gain switching must be realized in other parts of the circuit.**

Gain Switching in Inductively-Degenerated Cascode LNA: Two Approaches

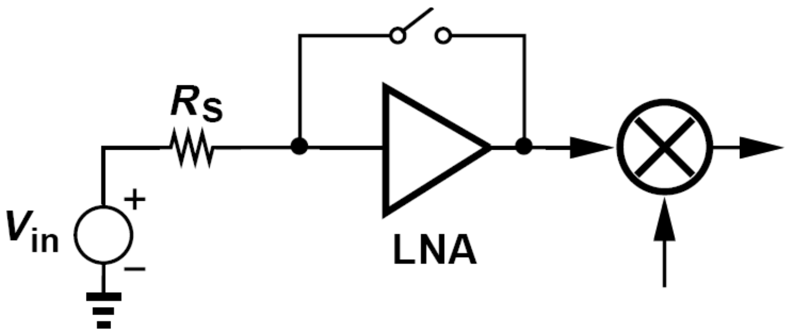
- The gain can be reduced by placing one or more PMOS switches in parallel with the load.
- Alternatively, the cascode switching scheme shown below (right) can be used.

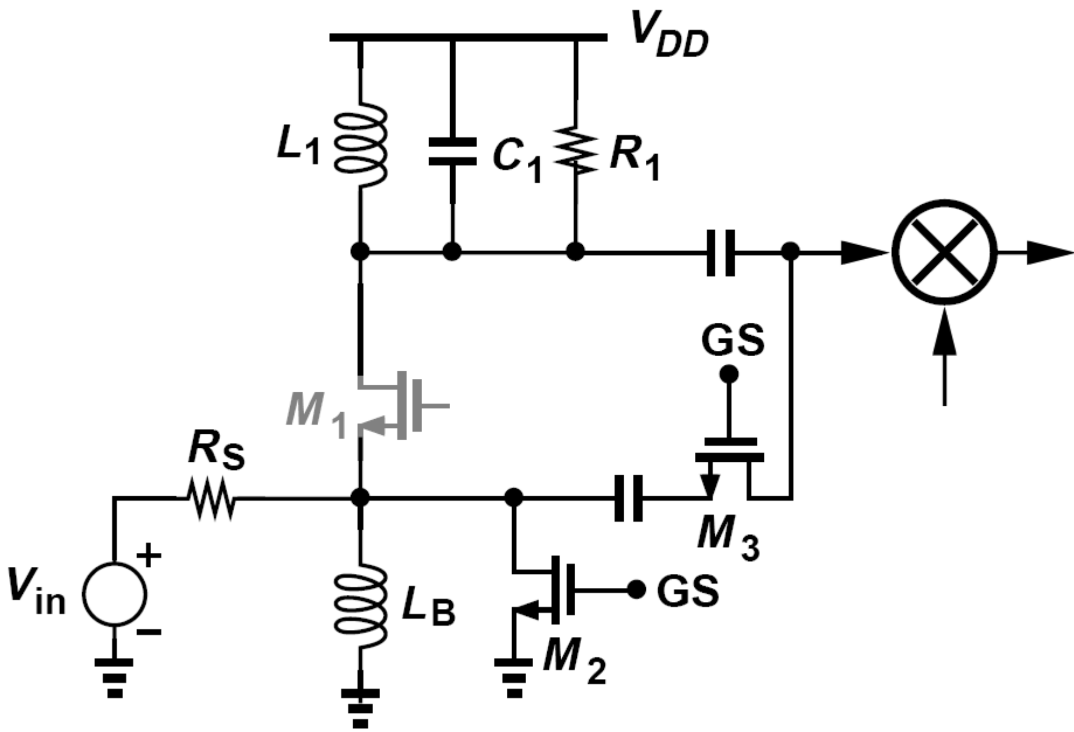


- Cascode switching is attractive because it reduces the current flowing through the load by a well-defined ratio and it negligibly alters the input impedance of the LNA.

LNA Bypass

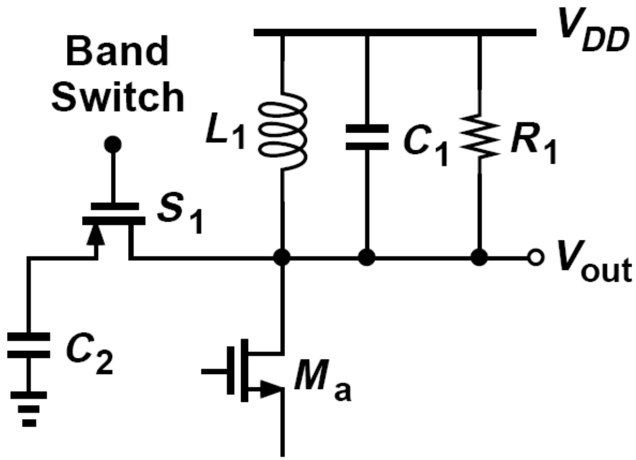
- **Receiver designs in which the LNA nonlinearity becomes problematic at high input levels can "bypass" the LNA in very-low-gain modes.**

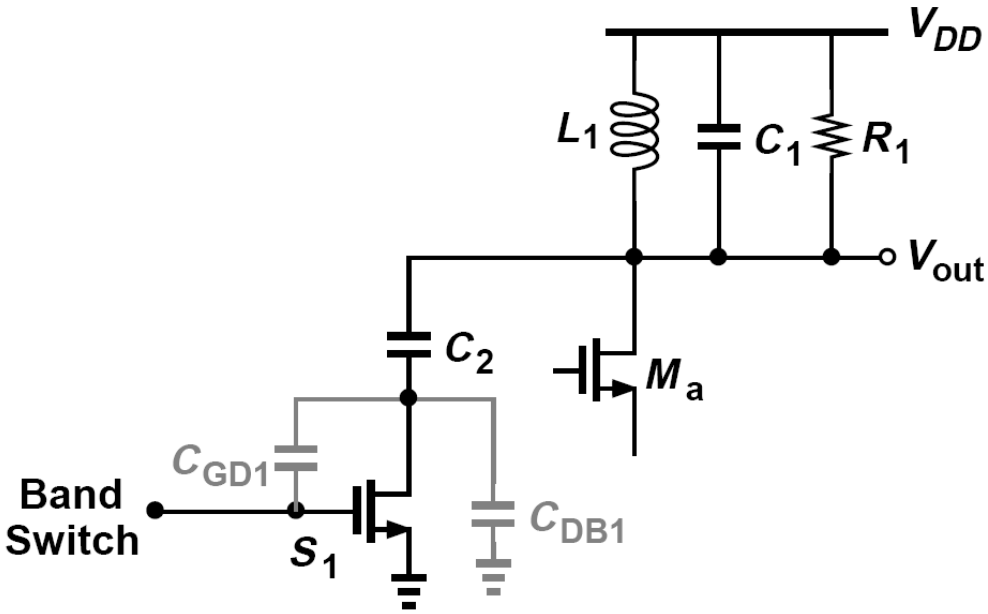




Band Switching

- LNAs that must operate across a wide bandwidth or in different bands can incorporate band switching.

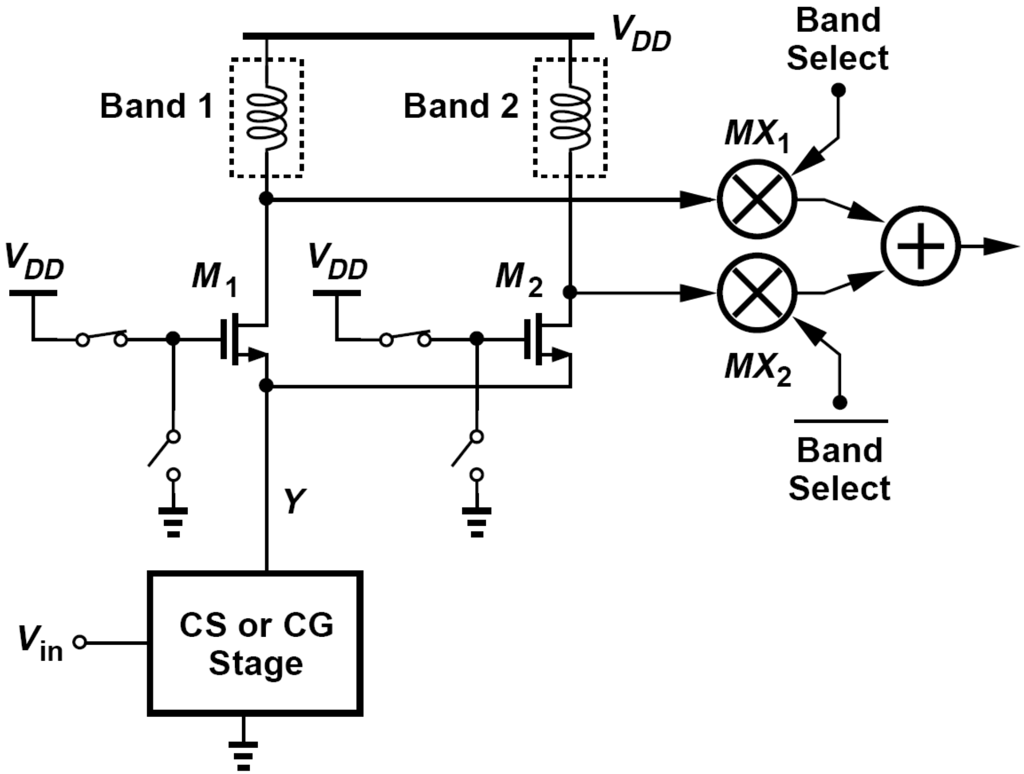




- We prefer the implementation above (right), where S_1 is formed as an NMOS device tied to ground.

Band Switching by Programmable Cascode Branches

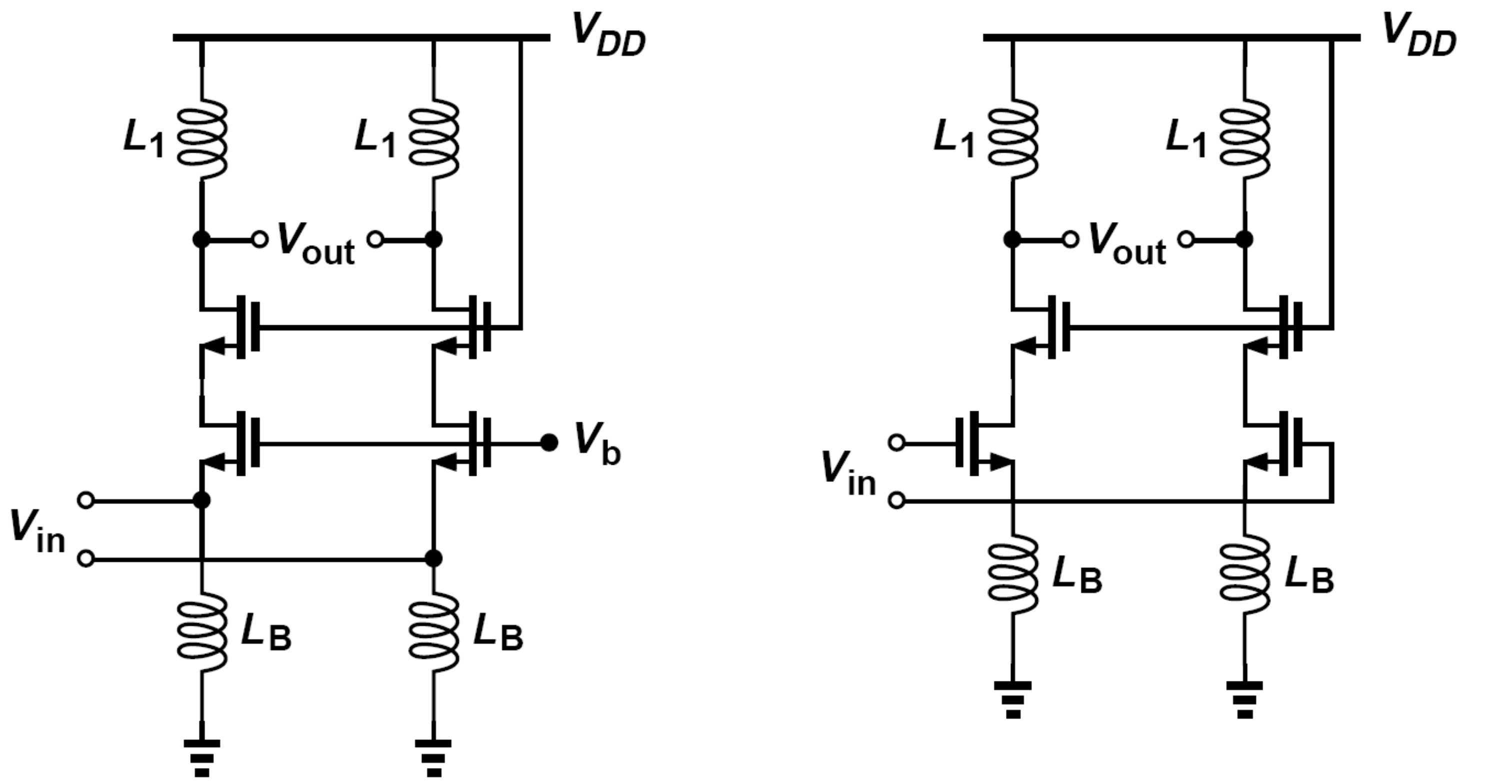
- An alternative method of band switching incorporates two or more tanks



- The principal drawback of this approach is the capacitance contributed by the additional cascode device(s) to node *Y*.
- Also, the spiral inductors have large footprints, making the layout and routing more difficult.

High-IP_2 LNAs: Differential LNAs

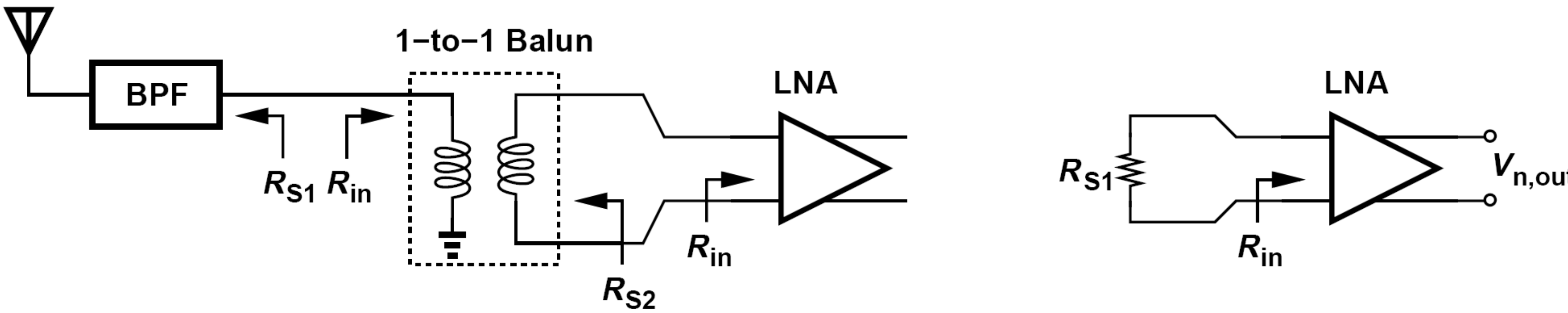
- **Differential LNAs can achieve high IP_2's because, symmetric circuits produce no even-order distortion.**



In principle, any of the single-ended LNAs studied thus far can be converted to differential form. Shown above are CG (left) and CS (right) stages.

Use of Balun at RX Input

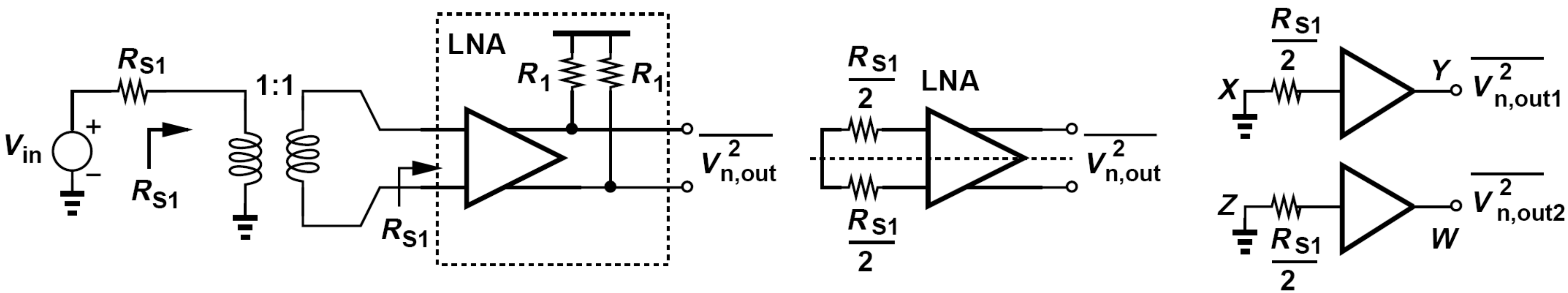
- Since the antenna and the preselect filter are typically single-ended, a transformer must precede the LNA to perform single-ended to differential conversion.



- The transformer is called a "balun," an acronym for "balanced-to-unbalanced" conversion because it can also perform differential to single-ended conversion if its two ports are swapped.
- Figure above (right) shows the setup for output noise calculation.

Differential CG LNA: Noise Figure

Assuming it is designed such that the impedance seen between each input node and ground is equal to $R_{S1}/2$



From the symmetry of the circuit that we can compute the output noise of each half circuit and add the output powers:

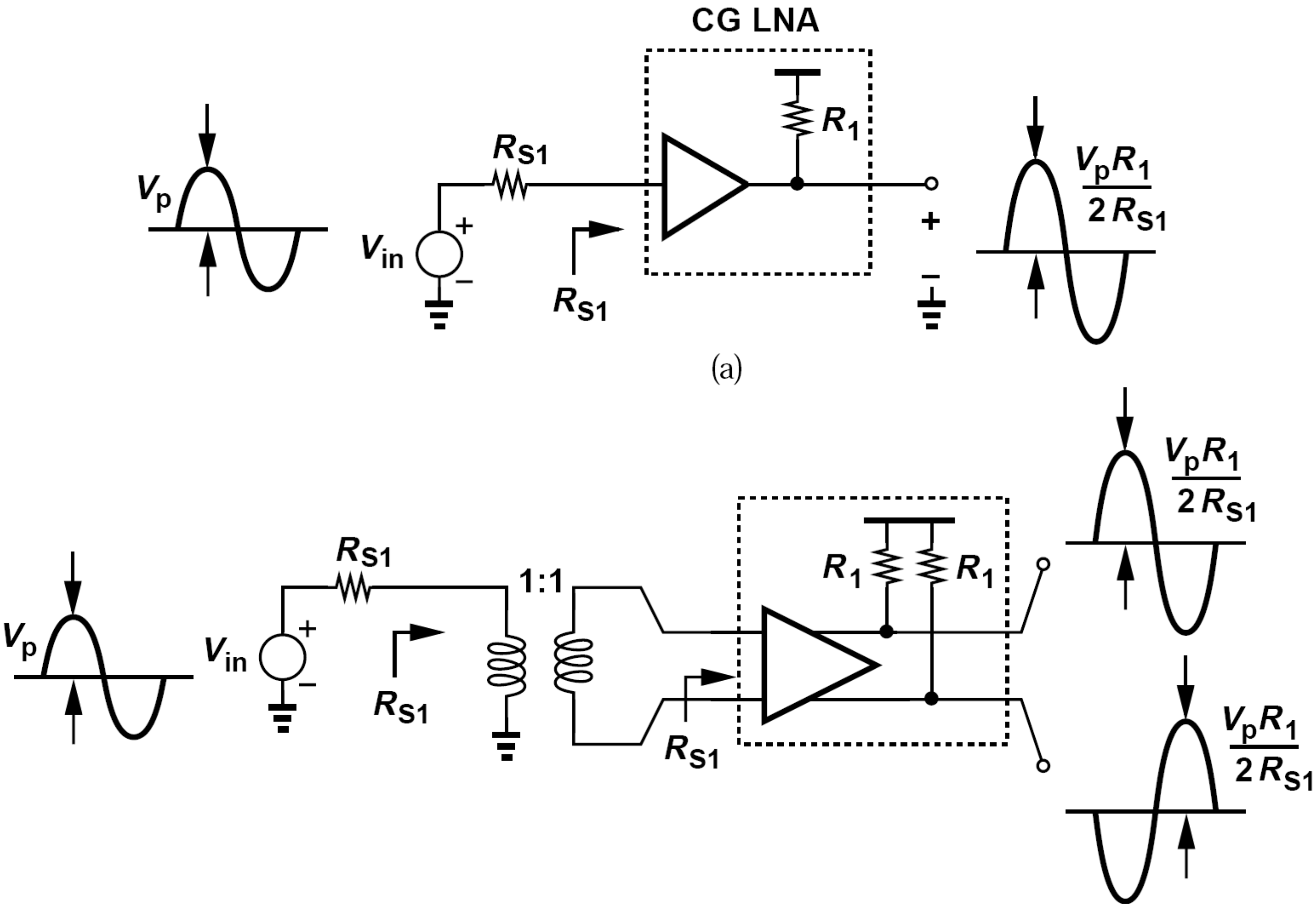
$$\overline{V^2_{n,out}} = \overline{V^2_{n,out1}} + \overline{V^2_{n,out2}}$$

$$\overline{V^2_{n,out1}} = kT\gamma\frac{R_1^2}{R_{S1}/2} + 4kTR_1 + 4kT\frac{R_{S1}}{2}\left(\frac{R_1}{\frac{2R_{S1}}{2}}\right)^2$$

$$\text{NF} = \frac{\overline{V^2_{n,out}}}{A_v^2}\cdot\frac{1}{4kTR_{S1}}$$

$$= 1+\gamma+\frac{2R_{S1}}{R_1}.$$

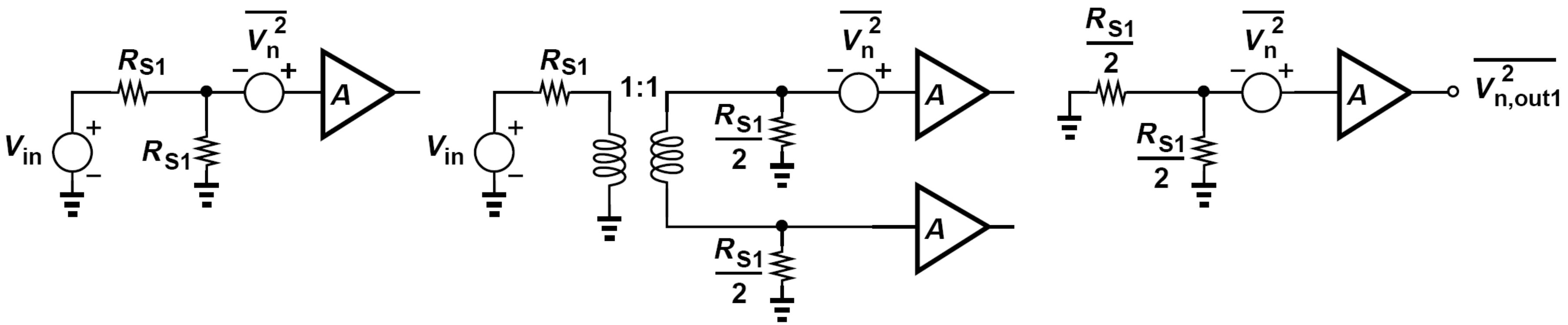
Comparison of Single-Ended and Differential CG LNAs



Voltage gain of differential CG LNA is twice that of the single ended one. On the other hand, the overall differential circuit contains two R_1's at its output, each contributing a noise power of $4kTR_1$.

Example of Differential Version and Noise Figure

An amplifier having a high input impedance employs a parallel resistor at the input to provide matching. Determine the noise figure of the circuit and its diff. version, shown below (middle), where two replicas of the amplifier are used.



Noise figure of the single-ended circuit:

$$\mathrm{NF}_{sing} = \frac{4kT\frac{R_{S1}}{2}A^2 + A^2\overline{V_n^2}}{\frac{A^2}{4}} \cdot \frac{1}{4kTR_{S1}}$$

$$= 2 + \frac{\overline{V_n^2}}{kTR_{S1}}.$$

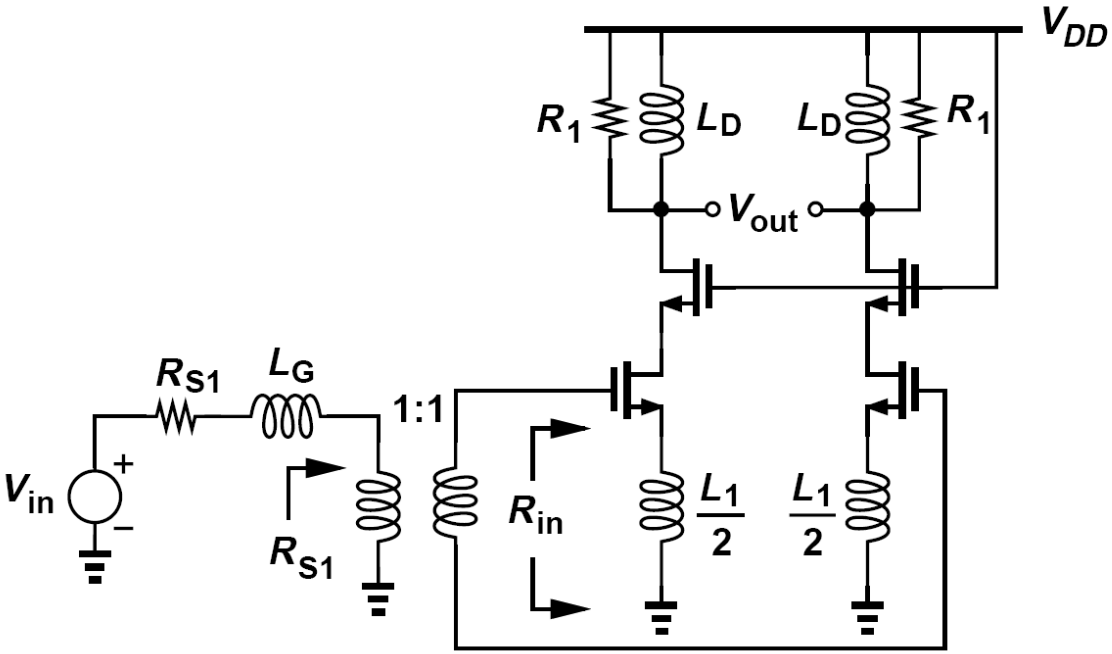
For the differential version:

$$\mathrm{NF}_{diff} = \frac{2\left(4kT\frac{R_{S1}}{4}A^2 + A^2\overline{V_n^2}\right)}{\frac{A^2}{4}} \cdot \frac{1}{4kTR_{S1}}$$

$$= 2 + \frac{2\overline{V_n^2}}{kTR_{S1}}.$$

Differential CS LNA

The differential CS LNA behaves differently from its CG counterpart.



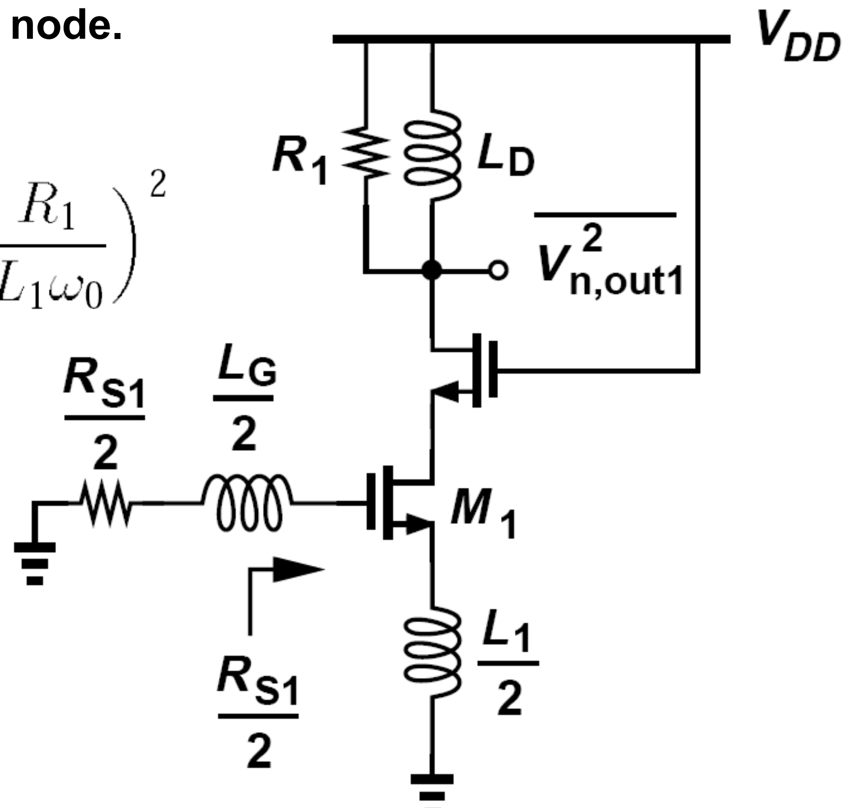
- **Recall that the input resistance of each half circuit is equal to $L_1\omega_T$ and must now be halved. This is accomplished by halving L_1.**
- **With input matching and a degeneration inductance of L_1, the voltage gain was found to be $R_1/(2L_1\omega_0)$, which is now doubled.**

Differential CS LNA: Noise Figure

Neglecting the contribution of the cascode device, if the input is matched, half of the noise current of the input transistor flows from the output node.

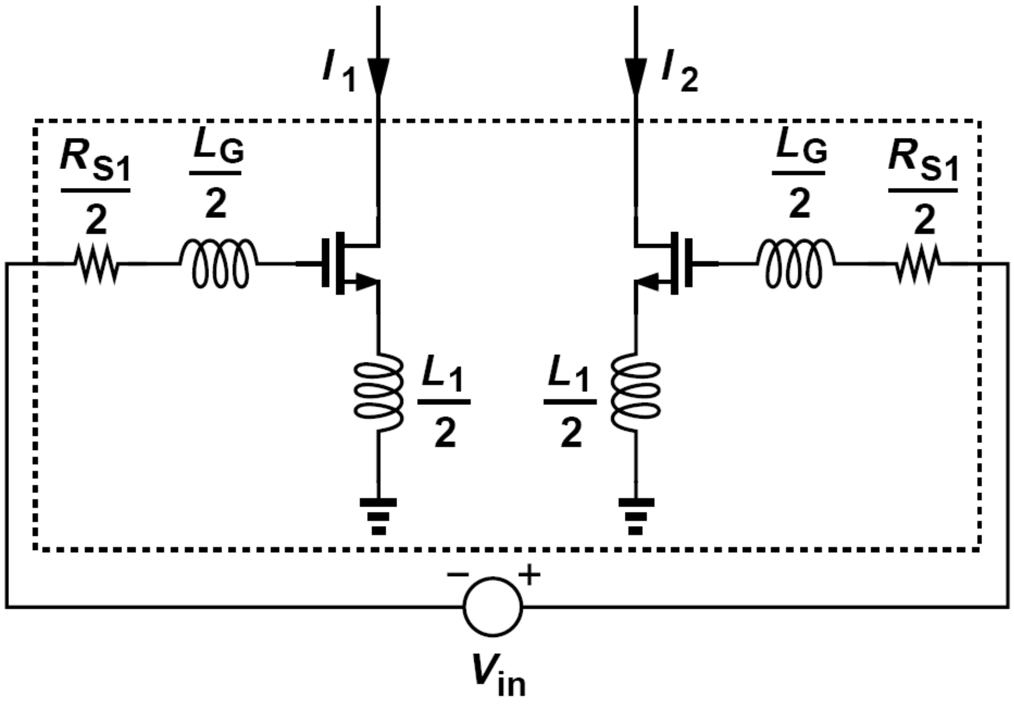
$$\overline{V^2_{n,out1}} = kT\gamma g_{m1}R_1^2 + 4kTR_1 + 4kT\frac{R_{S1}}{2}\left(\frac{R_1}{L_1\omega_0}\right)^2$$

$$\text{NF} = \frac{\gamma}{2}g_{m1}R_{S1}\left(\frac{\omega_0}{\omega_T}\right)^2 + \frac{2R_{S1}}{R_1}\left(\frac{\omega_0}{\omega_T}\right)^2 + 1.$$



Comparison with the Noise Figure of the Original Single-Ended LNA

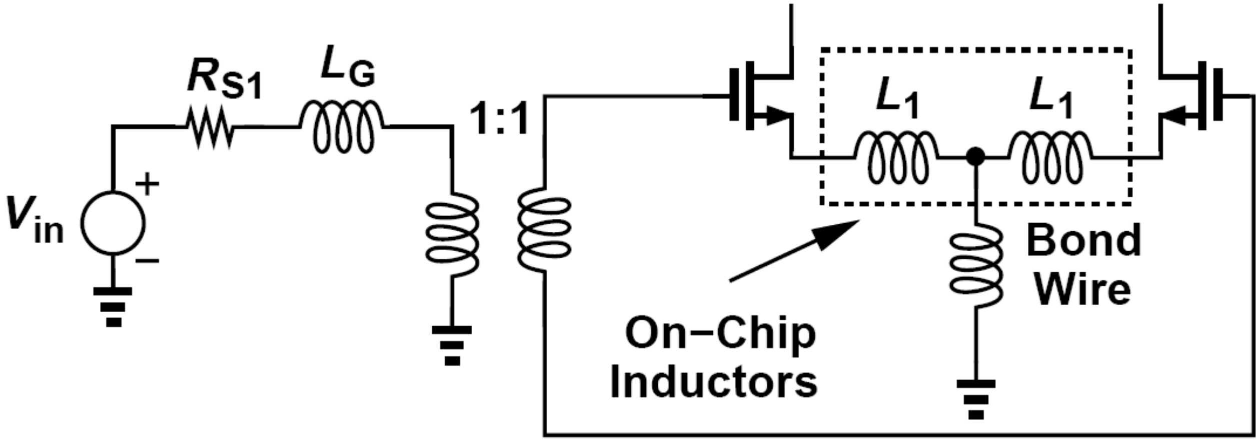
- **Compared with the Noise Figure of the Original Single-Ended LNA, both the transistor contribution and the load contribution are halved.**



- **However, this result holds only if the design can employ tow degeneration inductors, each having half the value of that in the single-ended counterpart.**

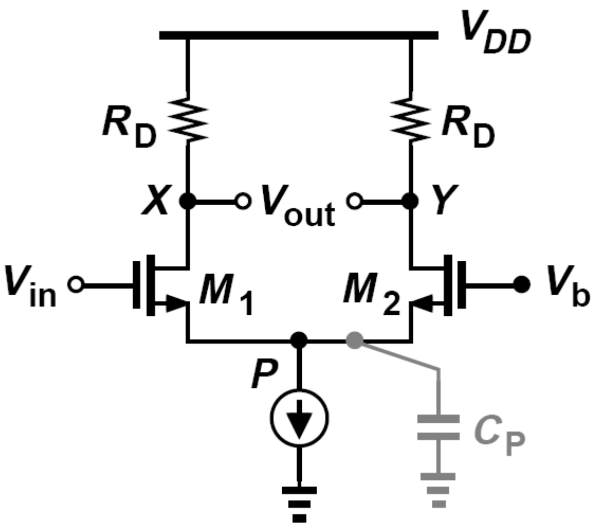
Differential CS Stage with On-Chip Degeneration Inductors

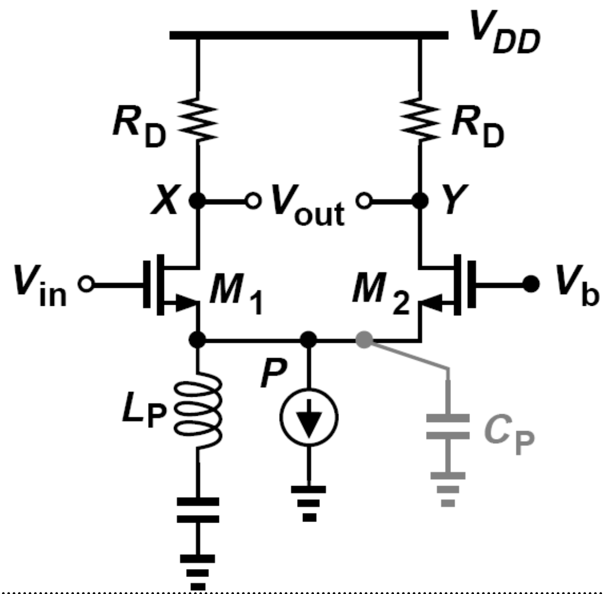
The design can incorporate on-chip degeneration inductors while converting the effect of the (inevitable) bond wire to a common-mode inductance.



- **The NF advantage implied previously may not materialize in reality because the loss of the balun is not negligible.**

Singe-Ended to Differential Conversion





- **At low to moderate frequencies, V_X and V_Y are differential and the voltage gain is equal to $g_{m1,2}R_D$.**
- **At high frequencies, however, two effects degrade the balance of the phases: the parasitic capacitance at node *P* and the gate-drain capacitance of M_1**

- **The capacitance at *P* can be nulled through the use of a parallel inductor, but the C_{GD1} feedforward persists.**

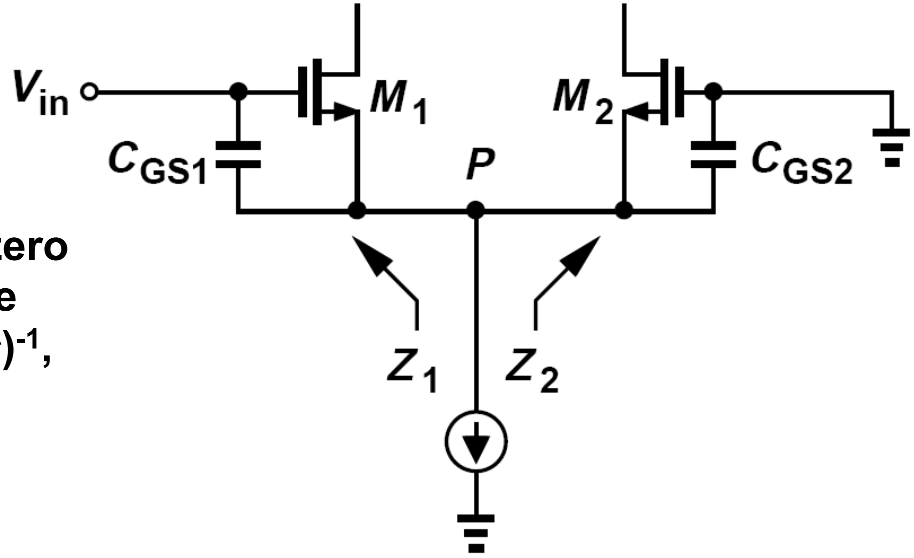
Example of Choice of L_P

A student computes C_P in previous figure as $C_{SB1} + C_{SB2} + C_{GS2}$, and selects the value of L_P accordingly. Is this an appropriate choice?

Solution:

No, it is not. For L_P to null the phase shift at P, it must resonate with only $C_{SB1}+C_{SB2}$. This point can be seen by examining the voltage division at node P. As shown below, in the absence of $C_{SB1} + C_{SB2}$,

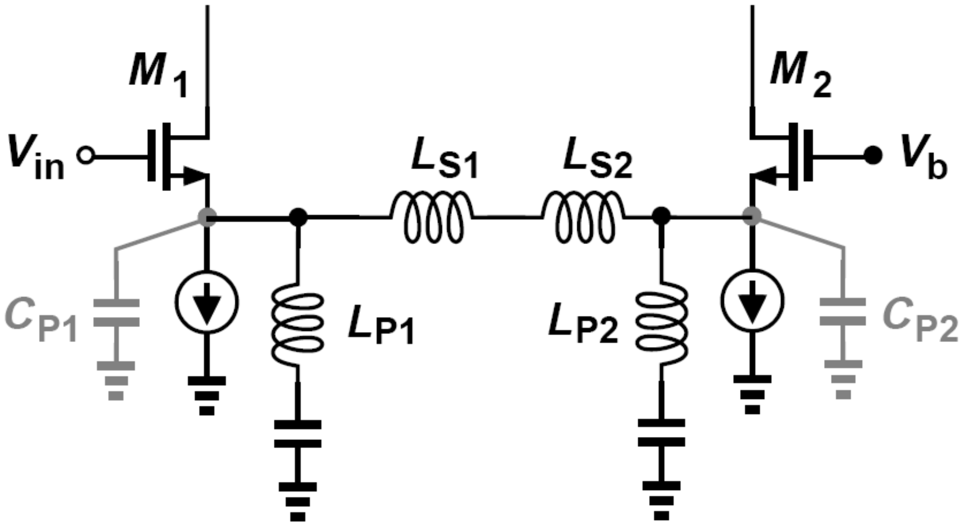
$$V_P = V_{in} \frac{Z_2}{Z_1 + Z_2}$$



For V_P to be exactly equal to half of V_{in} (with zero phase difference), we must have $Z_1 = Z_2$. Since each impedance is equal to $(g_m + g_{mb})^{-1} || (C_{GS}s)^{-1}$, we conclude that C_{GS2} must not be nulled.

Use of On-Chip Inductors for Resonance and Degeneration

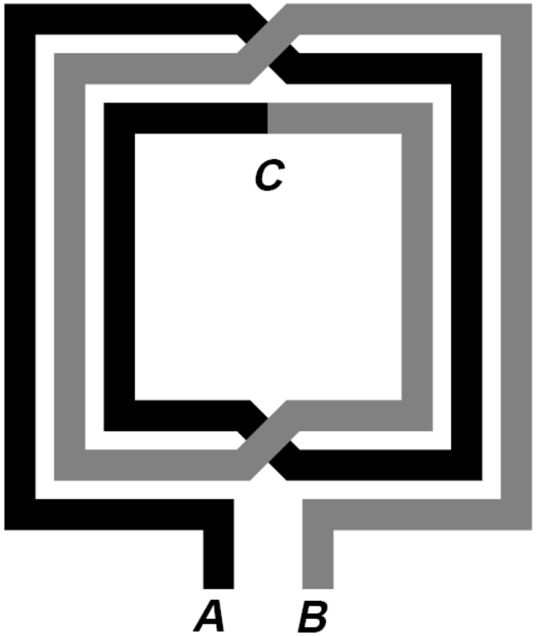
The topology discussed above still does not provide input matching. We must therefore insert (on-chip) inductances in series with the sources of M_1 and M_2.



- **Here, L_{P1} and L_{P2} resonate with C_{P1} and C_{P2}, respectively, and $L_{S1}+L_{S2}$ provides the necessary input resistance.**

Balun Issues

- External baluns with a low loss (e.g., 0.5 dB) in the gigahertz range are available from manufacturers, but they consume board space and raise the cost.
- Integrated baluns, on the other hand, suffer from a relatively high loss and large capacitances.



- The resistance and capacitance associated with the spirals and the sub-unity coupling factor make such baluns less attractive.

Use of 1-to-*N* Balun in an LNA

A student attempts to use a 1-to-*N* balun with a differential CS stage so as to amplify the input voltage by a factor of *N* and potentially achieve a lower noise figure. Compute the noise figure in this case.

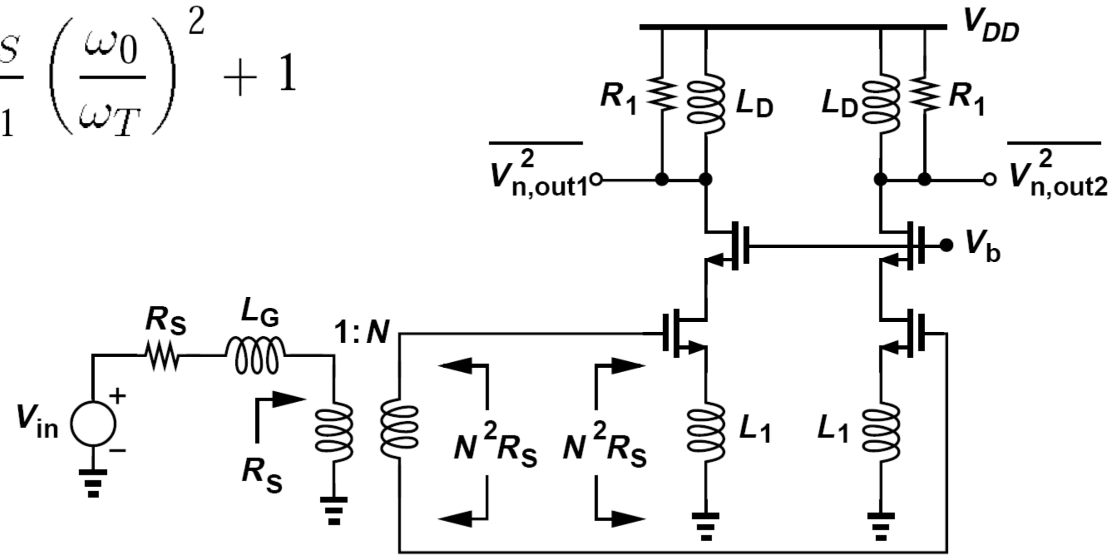
Since still half of the noise current of each input transistor flows to the output node, the noise power measured at each output is given by

$$\overline{V^2_{n,out1}} = \overline{V^2_{n,out2}} = 4kT\gamma g_{m1}\frac{R_1^2}{4} + 4kTR_1$$

The gain from V_{in} to the differential output is now equal to $NR_1/(2L_1\omega_0)$. Doubling the above power, dividing by the square of the gain, and normalizing to $4kTR_S$, we have

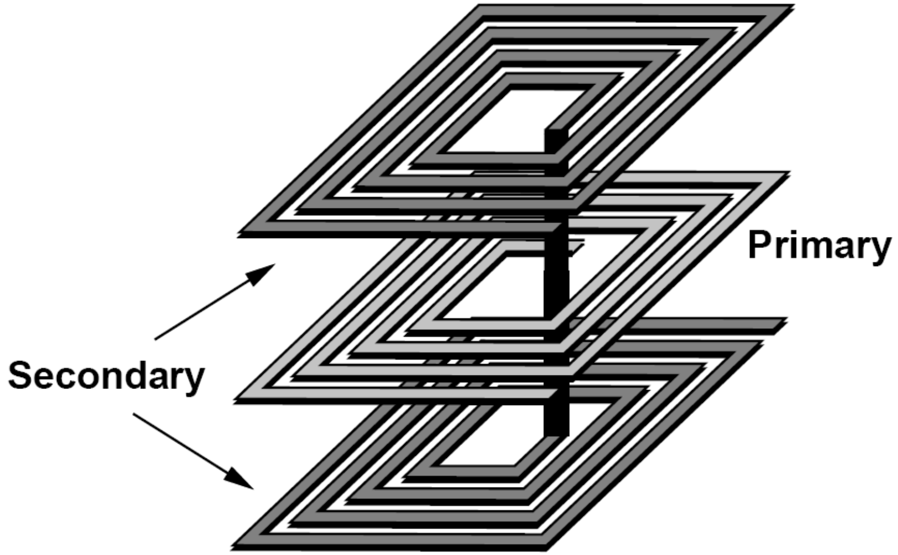
$$\mathrm{NF} = N^2\frac{\gamma}{2}g_{m1}R_S\left(\frac{\omega_0}{\omega_T}\right)^2 + 2N^2\frac{R_S}{R_1}\left(\frac{\omega_0}{\omega_T}\right)^2 + 1$$

We note, with great distress, that the first two terms have risen by a factor of N^2

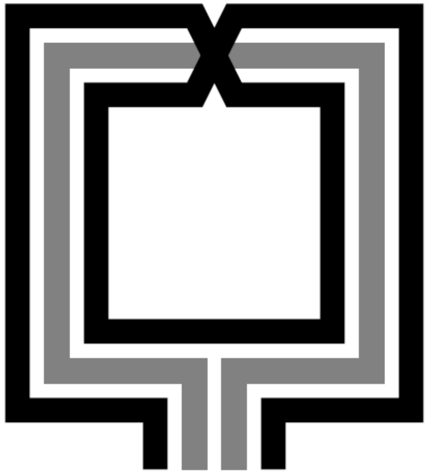


Realization of Baluns with Non-Unity Turns Ratio

- On-chip baluns with a non-unity turns ratio are difficult to design and suffer from a higher loss and a lower coupling factor.



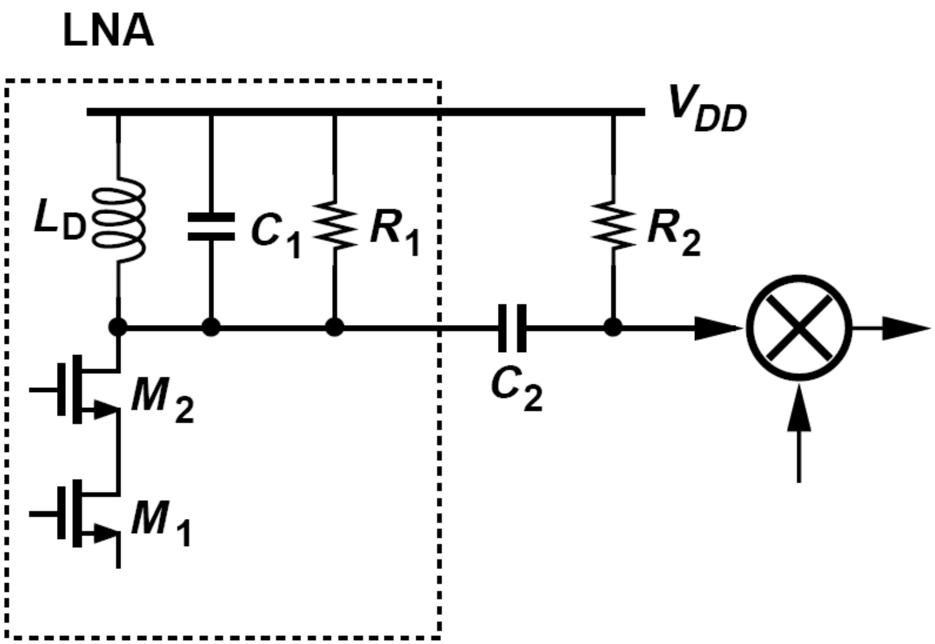
Stacked Spirals



Embedded Spirals

Other Methods of IP_2 Improvement

- **A possible approach to raising the IP_2 entails simply filtering the low-frequency second-order intermodulation product, called the beat component**



- **With this substantial suppression, the IP_2 of the LNA is unlikely to limit the RX performance, calling for techniques that improve the IP_2 of mixers.**

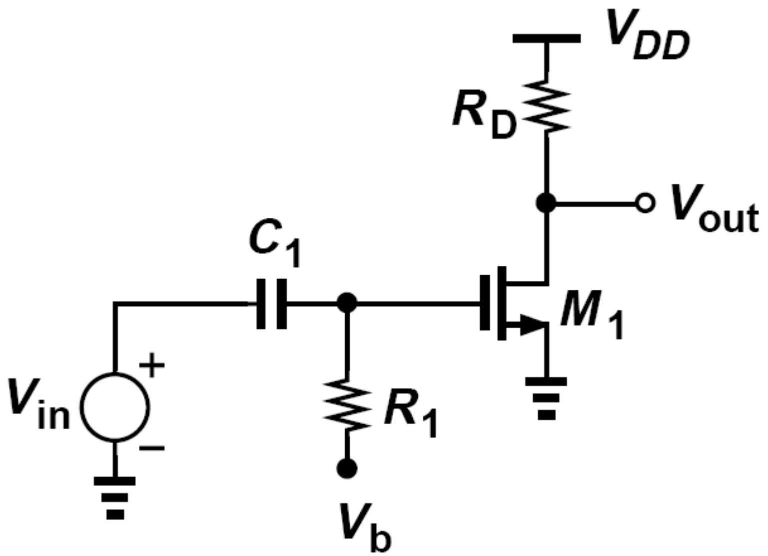
Nonlinearity Calculations

Systems with weak static nonlinearity can be approximated by a polynomial such as $y = \alpha_1 x + \alpha_2 x^2 + \alpha_3 x^3$. Let us devise a method for computing α_1-α_3 for a given circuit. In many circuits, it is difficult to derive y as an explicit function of x. However, we recognize that

$$\alpha_1 = \frac{\partial y}{\partial x}\Big|_{x=0}$$

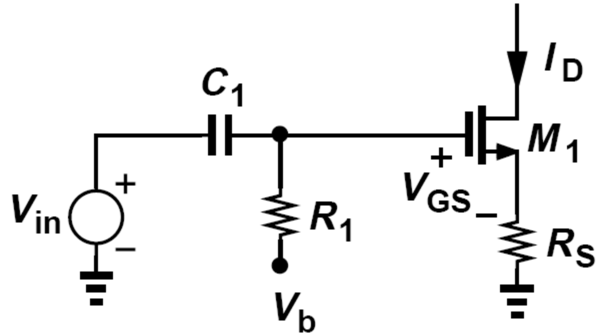
$$\alpha_2 = \frac{1}{2}\frac{\partial^2 y}{\partial x^2}\Big|_{x=0}$$

$$\alpha_3 = \frac{1}{6}\frac{\partial^3 y}{\partial x^3}\Big|_{x=0}.$$



- **It is important to note that in most cases, $x = 0$ in fact corresponds to the bias point of the circuit with no input perturbation.**

Degenerated CS Stage-IP_3 Calculation



For a simple square-law device

$$I_D = K(V_{GS} - V_{TH})^2$$

Since $V_{GS} = V_{in} - R_S I_D$,

$$I_D = K(V_{in} - R_S I_D - V_{TH})^2$$

Hence

$$\frac{\partial I_D}{\partial V_{in}} = 2K(V_{in} - R_S I_D - V_{TH})\left(1 - R_S \frac{\partial I_D}{\partial V_{in}}\right)$$

Also

$$\begin{aligned} g_m &= \frac{\partial I_D}{\partial V_{GS}} = 2K(V_{GS} - V_{TH}) \\ &= 2K(V_{in0} - R_S I_{D0} - V_{TH}) \end{aligned}$$

Thus, in the absence of signals

$$\frac{\partial I_D}{\partial V_{in}}|_{Vin0} = \alpha_1 = \frac{g_m}{1 + g_m R_S}$$

Degenerated CS Stage-IP$_3$ Calculation (Ⅱ)

We now compute the second derivative

$$\frac{\partial^2 I_D}{\partial V_{in}^2} = 2K\left(1 - R_S\frac{\partial I_D}{\partial V_{in}}\right)^2 + 2K(V_{in} - R_S I_D - V_{TH})\left(-R_S\frac{\partial^2 I_D}{\partial V_{in}^2}\right)$$

With no signals

$$\frac{\partial^2 I_D}{\partial V_{in}^2}|_{Vin0} = 2\alpha_2 = \frac{2K}{(1+g_m R_S)^3}$$

Lastly, we determine the third derivative

$$\begin{aligned}\frac{\partial^3 I_D}{\partial V_{in}^3} &= 4K\left(1 - R_S\frac{\partial I_D}{\partial V_{in}}\right)\left(-R_S\frac{\partial^2 I_D}{\partial V_{in}^2}\right) + 2K\left(1 - R_S\frac{\partial I_D}{\partial V_{in}}\right)\left(-R_S\frac{\partial^2 I_D}{\partial V_{in}^2}\right) \\ &- 2K(V_{in} - R_S I_D - V_{TH})R_S\frac{\partial^3 I_D}{\partial V_{in}^3},\end{aligned}$$

Which reduces to

$$\frac{\partial^3 I_D}{\partial V_{in}^3}|_{Vin0} = 6\alpha_3 = \frac{-12K^2 R_S}{(1+g_m R_S)^5}$$

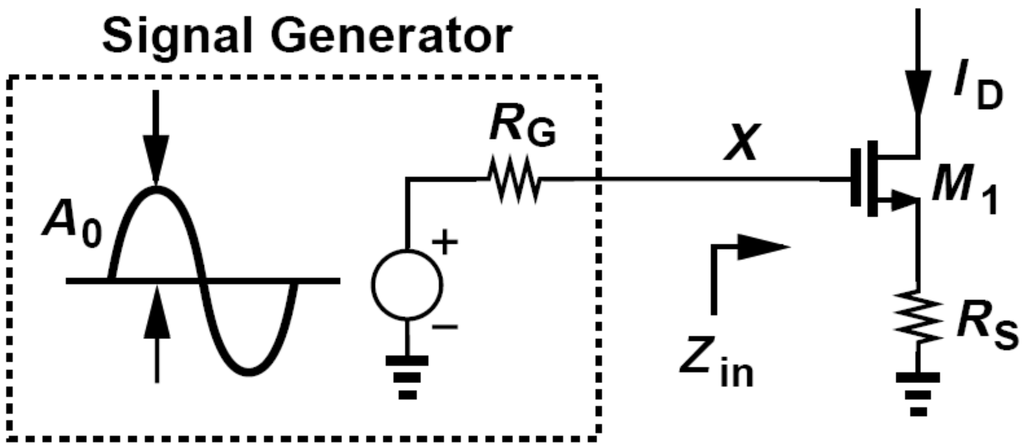
To compute the IP$_3$ of the stage, we write

$$\begin{aligned}A_{IIP3} &= \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \\ &= \sqrt{\frac{2g_m}{3R_S}\frac{(1+g_m R_S)^2}{K}}\end{aligned}$$

CS Stage Driven by Finite Signal Source Impedance

A student measures the IP_3 of the CS stage discussed above in the laboratory and obtains a value equal to half of that predicted by above equation. Explain why.

Solution:



The test setup is shown above, where the signal generator produces the required input. The discrepancy arises because the generator contains an internal output resistance R_G = 50 Ω, and it assumes that the circuit under test provides input matching, i.e., Z_{in} = 50 Ω. The generator's display therefore shows $A_0/2$ for the peak amplitude. The simple CS stage, on the other hand, exhibits a high input impedance, sensing a peak amplitude of A_0 rather than $A_0/2$. Thus, the level that the student reads is half of that applied to the circuit. This confusion arises in IP_3 measurements because this quantity has been traditionally defined in terms of the available input power.

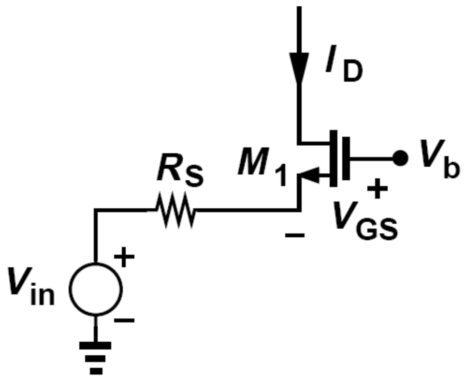
Example of IP_3 Calculation of a CG Stage

Compute the IP_3 of a common-gate stage if the input is matched. Neglect channel-length modulation and body effect.

$$I_D = K(V_b - V_{in} - I_D R_S - V_{TH})^2$$

Differentiating both sides with respect to V_{in} gives:

$$\frac{\partial I_D}{\partial V_{in}} = 2K(V_b - V_{in} - I_D R_S - V_{TH})\left(-1 - R_S \frac{\partial I_D}{\partial V_{in}}\right)$$



In the absence of signals

$$\frac{\partial I_D}{\partial V_{in}}|_{Vin0} = \frac{-g_m}{1 + g_m R_S}$$

The second derivative is identical to that of the CS stage

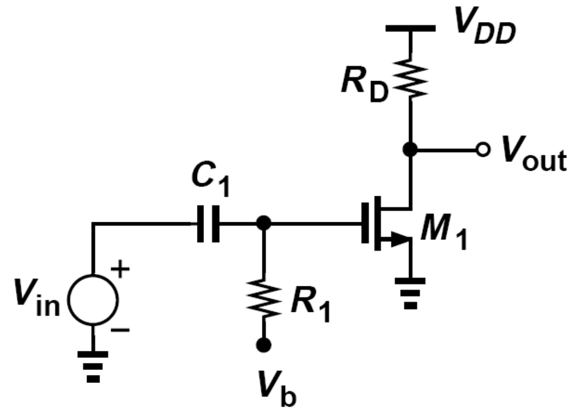
$$\frac{\partial^2 I_D}{\partial V_{in}^2}|_{Vin0} = \frac{2K}{(1 + g_m R_S)^3}$$

and the third derivative emerges as

$$\frac{\partial^3 I_D}{\partial V_{in}^3}|_{Vin0} = \frac{12K^2 R_S}{(1 + g_m R_S)^5}$$

$$\begin{aligned} A_{IIP3} &= \frac{2}{K}\sqrt{\frac{2}{3}} g_m \\ &= 4\sqrt{\frac{2}{3}}(V_{GS0} - V_{TH}) \end{aligned}$$

Undegenerated CS Stage: IP_3 Calculation (Ⅰ)



The effect of mobility degradation due to both vertical and lateral fields in the channel can be approximated as:

$$I_D = \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}\frac{(V_{GS}-V_{TH})^2}{1+(\frac{\mu_0}{2v_{sat}L}+\theta)(V_{GS}-V_{TH})}$$

And

$$I_D \approx \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}\left[(V_{GS}-V_{TH})^2-\left(\frac{\mu_0}{2v_{sat}L}+\theta\right)(V_{GS}-V_{TH})^3\right]$$

Replace V_{GS} with V_{in} + V_{GS0}, obtaining

$$\begin{aligned} I_D &\approx K[2-3a(V_{GS0}-V_{TH})](V_{GS0}-V_{TH})V_{in}+K[1-3a(V_{GS0}-V_{TH})]V_{in}^2 \\ &- KaV_{in}^3+K(V_{GS0}-V_{TH})^2-aK(V_{GS0}-V_{TH})^3, \end{aligned}$$

It follows that

$$\begin{aligned} \alpha_1 &= K[2-3a(V_{GS0}-V_{TH})](V_{GS0}-V_{TH}) \\ \alpha_3 &= -Ka. \end{aligned}$$

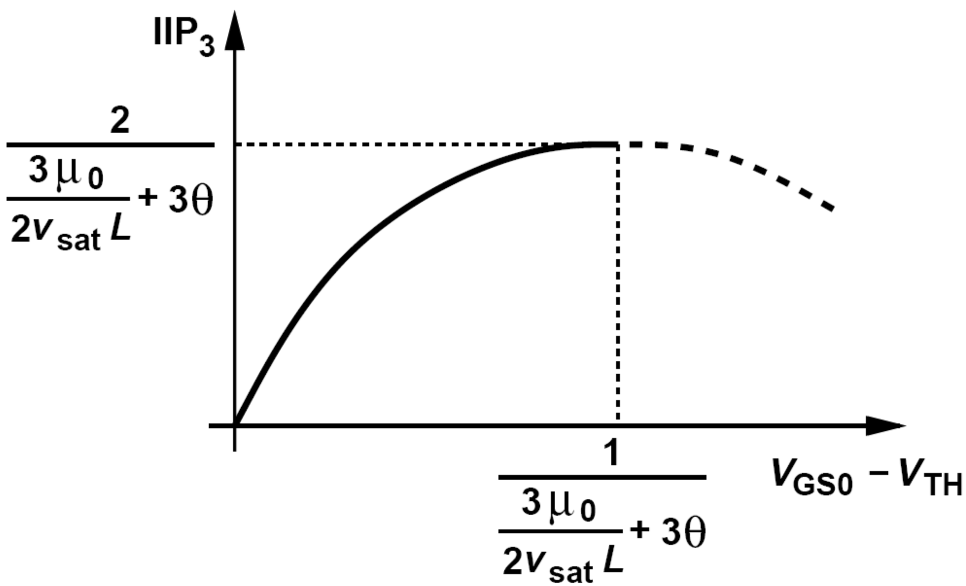
Undegenerated CS Stage: IP_3 Calculation (Ⅱ)

$$A_{IIP3} = \sqrt{\frac{4}{3} \times \frac{2 - 3a(V_{GS0} - V_{TH})}{a}(V_{GS0} - V_{TH})}$$

$$= \sqrt{\frac{\frac{8}{3}(V_{GS0} - V_{TH})}{\frac{\mu_0}{2v_{sat}L} + \theta} - 4(V_{GS0} - V_{TH})^2}.$$

We note that the *IP_3* rises with the bias overdrive voltage, reaching a maximum of

$$A_{IIP3,max} = \frac{2}{3a} = \frac{2}{3}\frac{1}{\frac{\mu_0}{2v_{sat}L} + \theta}$$



Calculation with Another Approximation

If the second term in the denominator of previous approximation of I_D is only somewhat less than unity, a better approximation must be used, e.g., $(1 + \varepsilon)^{-1} \approx 1 - \varepsilon + \varepsilon^2$. Compute α_1 and α_3 with this approximation.

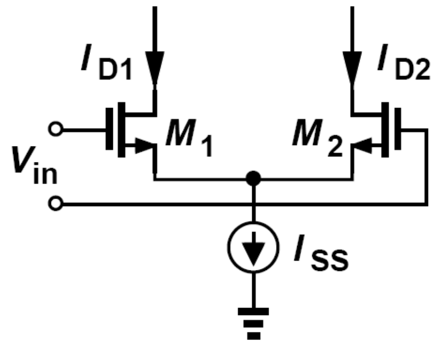
Solution:

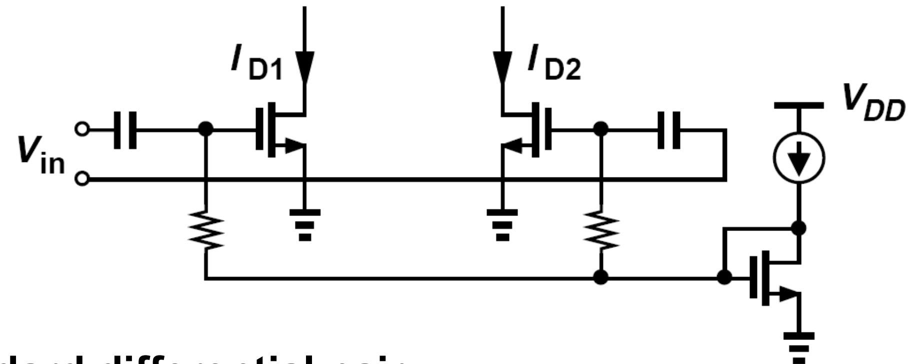
The additional term $a^2(V_{GS} - V_{TH})^2$ is multiplied by $K(V_{GS} - V_{TH})^2$, yielding two terms of interest: $4Ka^2V_{in}(V_{GS} - V_{TH})^3$ and $4Ka^2V_{in}^3(V_{GS} - V_{TH})$. The former contributes to α_1 and the latter to α_3. It follows that

$$\alpha_1 = K[2 - 3a(V_{GS0} - V_{TH}) + 4a^2(V_{GS0} - V_{TH})^2](V_{GS0} - V_{TH})$$

$$\alpha_3 = -Ka[1 - 4a(V_{GS0} - V_{TH})].$$

Differential and Quasi-Differential Pairs





We study the nonlinearity of the standard differential pair

$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{in}\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - V_{in}^2},$$

If $|V_{in}| << I_{SS}/(\mu_n C_{ox} W/L)$, then

$$I_{D1} - I_{D2} \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{in}\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}\left(1 - \frac{1}{2}\frac{V_{in}^2}{\frac{4I_{SS}}{\mu_n C_{ox}W/L}}\right)$$

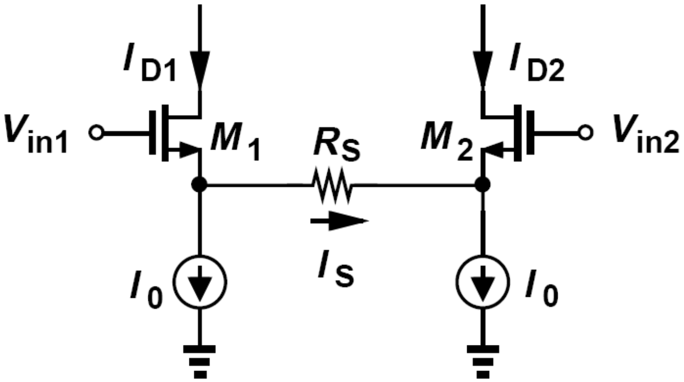
$$\alpha_1 = \sqrt{\mu_n C_{ox}\frac{W}{L}I_{SS}}$$

$$\alpha_3 = -\left(\mu_n C_{ox}\frac{W}{L}\right)^{3/2}\frac{1}{8\sqrt{I_{SS}}}$$

$$\Rightarrow \quad A_{IIP3} = \sqrt{\frac{6I_{SS}}{\mu_n C_{ox}W/L}} = \sqrt{6}(V_{GS0} - V_{TH})$$

Degenerated Differential Pair

Consider the circuit shown on the right, we have:



$$V_{in} - R_S I_{D1} + R_S I_0 = \frac{1}{\sqrt{K}}(\sqrt{I_{D1}} - \sqrt{I_{D2}})$$

Differentiating both sides with respect to *V_{in}* yields

$$\frac{\partial I_{D1}}{\partial V_{in}} \left[R_S + \frac{1}{2\sqrt{K}} \left(\frac{1}{\sqrt{I_{D1}}} + \frac{1}{\sqrt{I_{D2}}} \right) \right] = 1$$

At *V_{in}* = 0, *I_{D1}* = *I_{D2}* and $\alpha_1 = \dfrac{1}{R_S + \dfrac{2}{g_m}}$

Differentiating again gives:

$$\frac{\partial^2 I_{D1}}{\partial V_{in}^2} \left[R_S + \frac{1}{2\sqrt{K}} \left(\frac{1}{\sqrt{I_{D1}}} + \frac{1}{\sqrt{I_{D2}}} \right) \right] - \frac{\partial I_{D1}}{\partial V_{in}} \left[\frac{1}{4\sqrt{K}} \left(\frac{1}{I_{D1}^{3/2}} \frac{\partial I_{D1}}{\partial V_{in}} + \frac{1}{I_{D2}^{3/2}} \frac{\partial I_{D2}}{\partial V_{in}} \right) \right] = 0$$

Differentiating once more gives:

$$\frac{\partial^3 I_{D1}}{\partial V_{in}^3}\bigg|_{Vin=0} = \frac{-3}{(R_S + \frac{2}{g_m})^4 g_m I_0^2} = 6\alpha_3$$

$$A_{IIP3} = \frac{2I_0}{3}\sqrt{g_m \left(R_S + \frac{2}{g_m} \right)^3}$$